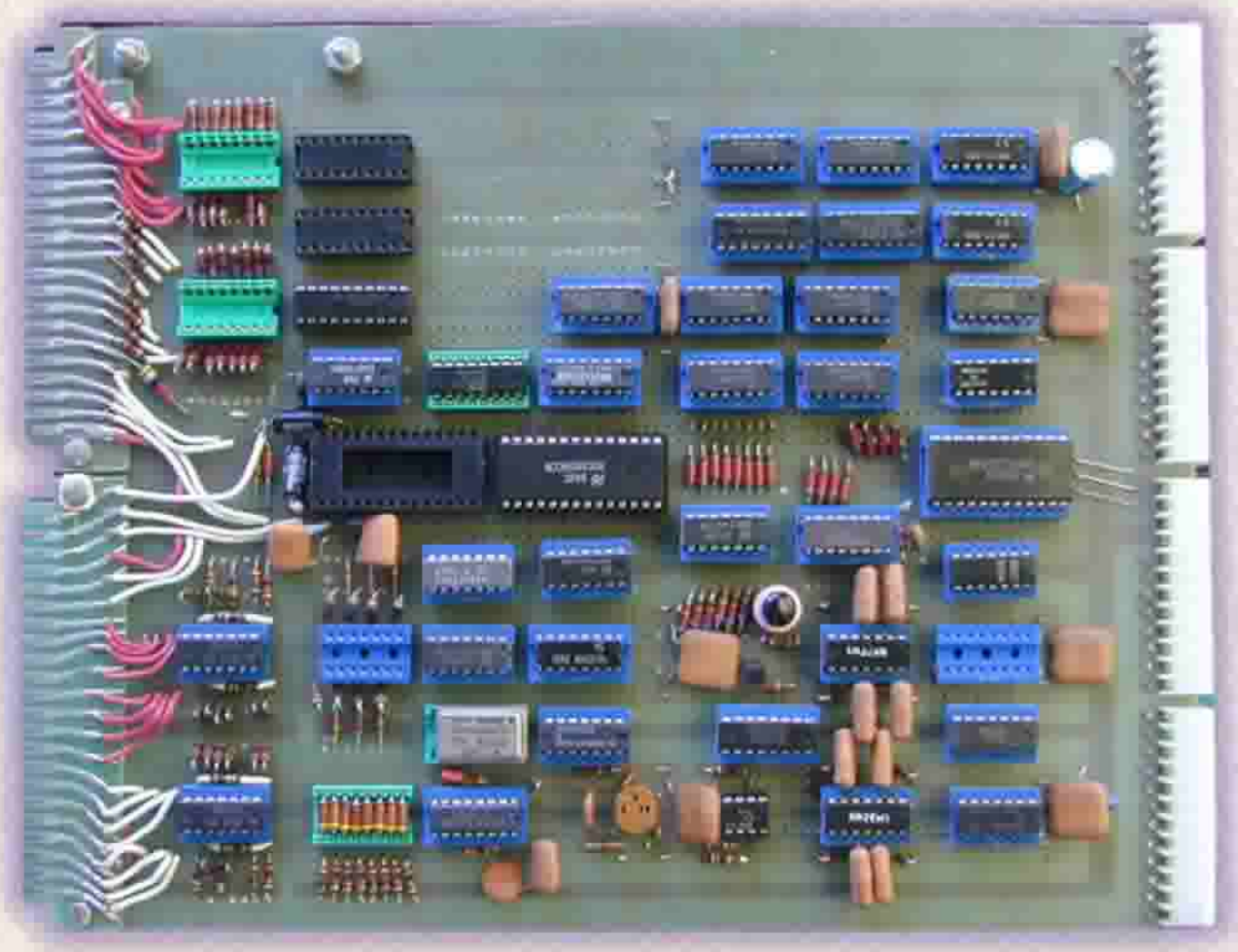


Ohio Scientific Micro Devices

OSI PULSE GENERATOR, PULSE DETECTOR

There are 8 pulse outputs. Each output is associated with one bit of the 8-bit data word at micro address 32,785 (8011 Hex.).

PULSE #	7	6	5	4	3	2	1	0
DATA BIT #	**7**	6	5	4	3	2	1	0
BIT VALUE	128	64	32	16	8	4	2	1

To generate a pulse the associated bit at location 32785 must be turned on (1) with a memory write operation. For example, to generate Pulses #5 and #3 simultaneously, write a 40 (32+8 in decimal, 0010 1000 in binary, 28 in hexadecimal) into address 32785 (8011 hex). A 12 volt, 0.6 millisecond pulse will then result at Pulse Outs #5 and #3.

PULSE IN#	7	6	5	4	3	2	1	0
DATA BIT#	7	6	5	4	3	2	1	0
BIT VALUE	128	64	32	16	8	4	2	1

A pulse occurring at one of the pulse inputs will automatically turn on the associated bit at location 32784. The memory location can be read to see which inputs received pulses since the last read operation. After each read operation the 8-data bits are automatically cleared to zero again.

For example, suppose a pulse occurs at pulse inputs #6 and #3. If memory location 32784 is then read, the number 72 (64+8 in decimal, 0100 1000 in binary, 48 in hexadecimal) will be found there. If location 32784 is immediately read again the number 0 will be found, showing that the read operation did result in clearing the word.

The pulse detector also has interrupt capabilities. Whenever one or more of address 32784's data bits are on (1), then the microcomputer's IRQ interrupt request line is pulled low,The IRQ line returns high when the pulse detect address is cleared again by a read operation.

Any number of devices can pull the IRQ line low, the Hybrid being one of them. Address location 32771 (8003_{Hex}) is set up to enable the user to determine which device is requesting an interrupt, The Most Significant Bit is assigned to the Hybrid Synthesizer, and the Least Significant Bit is assigned to the Pulse Detector. If the bit is on (1), then that device is the interrupting device. Note that this is also a means of detecting a pulse occurrence without clearing the pulse detector address location.

The IRQ interrupt request line is normally masked by the 'I' bit of the 6502 processor status register being set to 1. Entering BASIC automatically sets this bit. It can also be set by the SEI machine code instruction or by loading 04_{Hex} into location $O12C_{Hex}$ (the Monitor Program's Go and Break-point location for the Status Register),

When the IRQ Mask Bit I in the 6502 Status Register is cleared to 0, the interrupt routine is enabled. When the IRQ line goes low the Microcomputer stops whatever it is doing in order to service the interrupt. It will go to the address $01C0_{Hex}$ (448_{Dec}) expecting to find there a user loaded subroutine to deal with the interrupt.

OSI DIGITAL TO ANALOG CONVERTERS (DAC)

There are 8 DACs found at micro address locations 32800 through 32807 (8020 to 8027 Hex). The 8-bit data word written into one of these address locations is converted to a voltage level appearing at one of the front panel's 8 DAC output jacks.

Note that the DACs use only the Write function of the address locations. Reading into the same locations will access the ADCs, not the DACs.

An 8-bit data word provides for 256 possible voltage levels at the DAC output. As the data word is incremented from zero to 255 the output voltage goes from zero volts to some maximum. The maximum voltage is set by a DAC volume control which affects all 8 DACs simultaneously. Thus the maximum voltage can be varied from about 2 volts to 12 volts. The step size also changes by the value Vmax/255

The 8 DACs are actually multiplexed. That is, one converter is used to convert the 8 digital input words one at a time. The result is held in a sample-and-hold circuit until the converter comes back around to that one input word again. This, of course, is done at a high speed - one conversion takes 4 microseconds. The sampling rate for each output is 31.25 KHz. Thus the DACs can handle audio signals as high as about 15 KHz.

OSI ANALOG TO DIGITAL CONVERTERS (ADC)

There are 8 ADCs found at micro address locations 32800 through 32807 (8020 to 8027 Hex). The 8-bit data word read from one of these address locations is derived from the voltage appearing at one of the front panel's 8 ADC input jacks.

Note that the ADCs use only the Read function of the address locations. Writing into the same locations will access the DACs, not the ADCs.

The ADCs accept voltage input levels from zero to 5 volts. A zero volt input is converted into a zero value 8-bit word. Any voltages lower than zero volts are also converted to the zero value. A 5 volt input level is converted to the number 255. Any voltages above 5 volts are also converted as 255.

The input to each ADC has been designed with an AC/DC switch in order to accomodate both signal and control voltage inputs. Also, an attenuator control has been placed on each input so that one can adjust for the 0 to 5 volt input limitations. The input circuitry works as follows:

1) with no signal input and the input switch on 'CV' The Attenuator control acts as a variable voltage from 0 to 5 volts,

2) with a Control Voltage input and the input switch on 'CV' the actual signal going to the ADC is an attenuated Control Voltage. The Control pot should be adjusted so that 255 is read with the maximum CV input.

3) With a Signal input and the input switch on 'SIG' the actual signal going to the ABC is an attenuated signal offset to 2.5 volts. The output values read, then, vary around the bias value 127.

The 8 ADCs are actually multiplexed. That is, one converter is used to convert all 8 inputs one at a time in succession. Since the ADC used is relatively slow this multiplexing scheme severely limits the frequency range the ADC can handle. A compromised solution to this problem has been worked out. It centers around the 3-position switch marked '8 4 2'. In the '8' position, all 8 inputs are converted at the slowest sampling speed and thus the most severe frequency input limit. In the '4' position, only ADC inputs 0, 1, 2, 3 are converted at twice the sampling rate. Finally, in the '2' position, only ADC inputs 0 and 1 are converted at 4 times the sampling rate.

The chart below shows the resulting high frequency limitations for each of the 3 switch settings. It is based on a single conversion time of 125 microseconds,

SWITCH POSITION	INPUTS CONVERTED	SAMPLING FREQUENCY	MAXIMUM INPUT FREQUENCY
2	0,1	4KHz	2KHz
4	0, 1, 2, 3	2 KHz	1KHz
8	All 8	1KHz	500 Hz

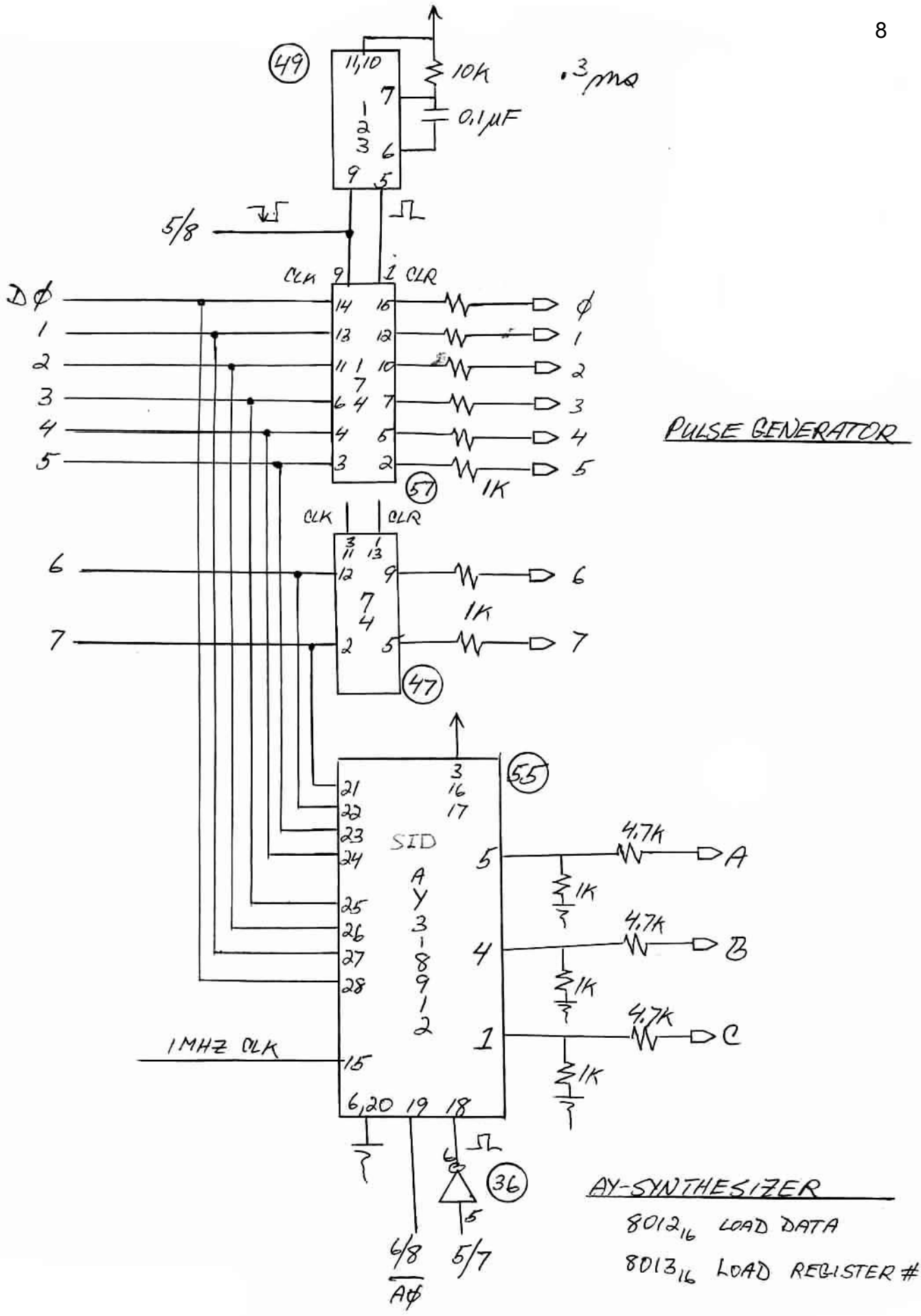
AY-3-8912 PROGRAMMABLE SOUND GENERATOR

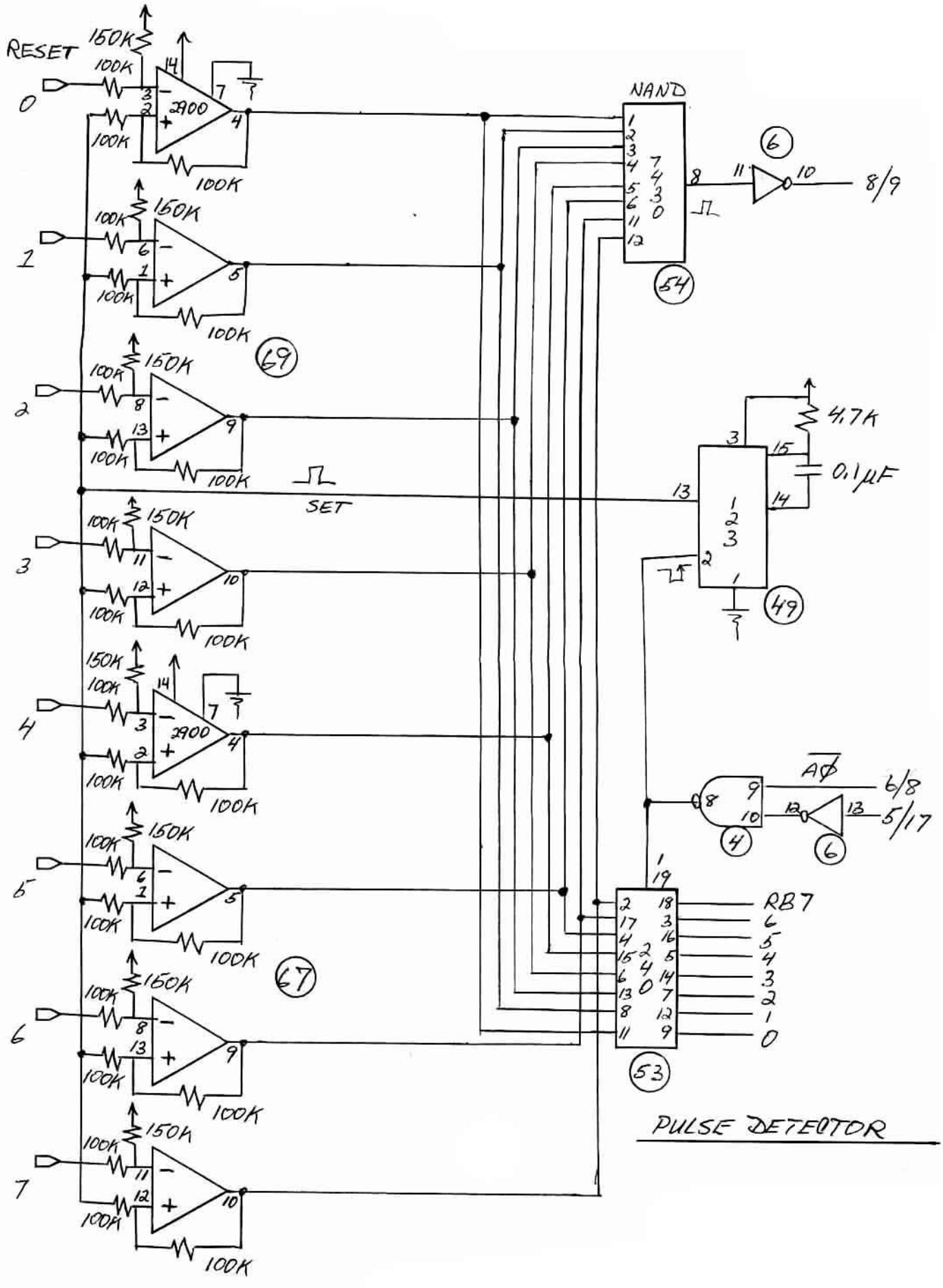
The AY-3-8912 PSG is a Large Scale Integrated Circuit Chip which can produce a variety of complex sounds under software control. The chip has three 1-volt peak-to-peak square wave signal outputs. The user can control the pitch, amplitude, tone/noise mix, and envelope of these outputs.

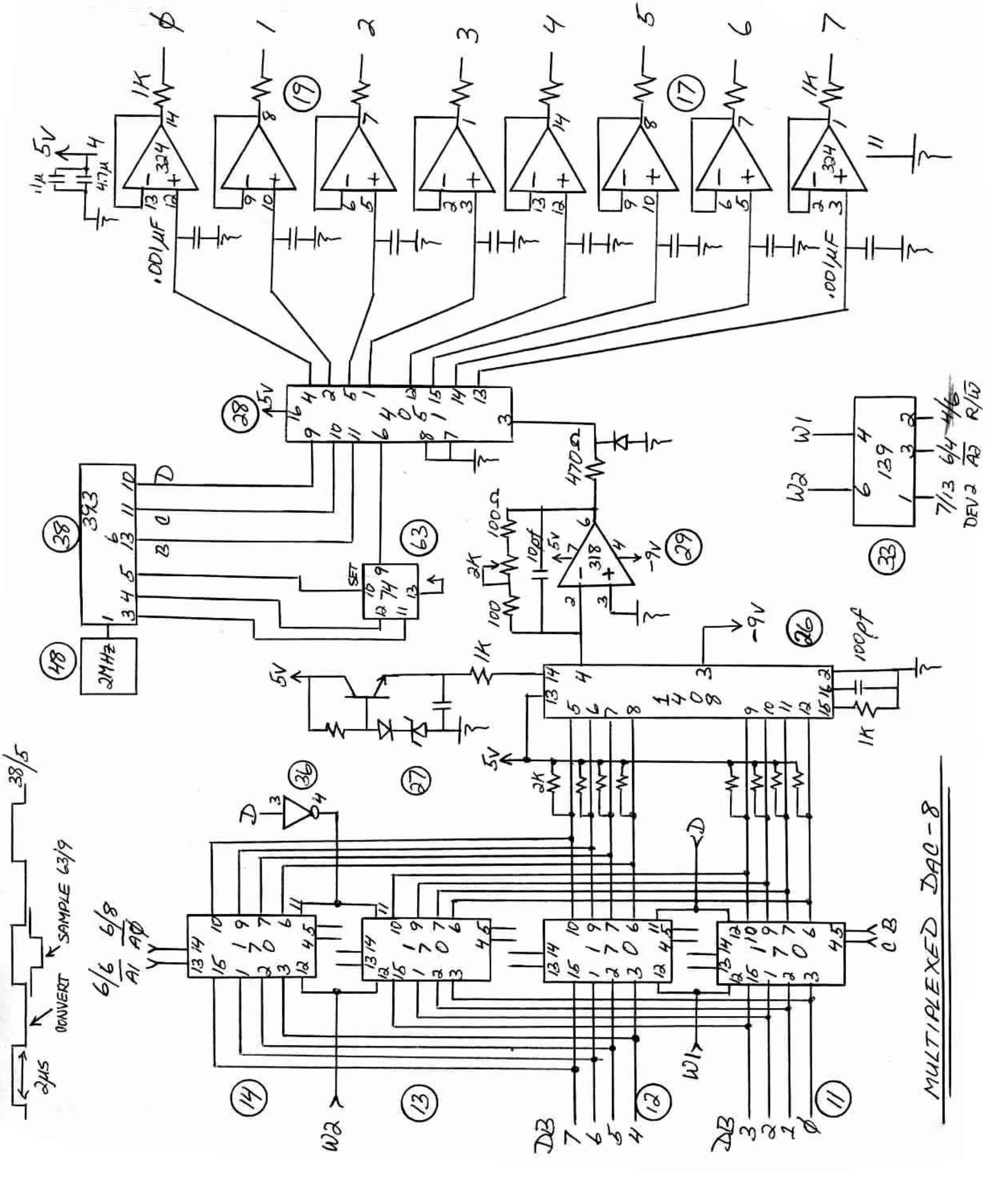
The chip contains 16 data registers which the user loads to control the various sound parameters. These 16 registers are entered via two micro address ports.

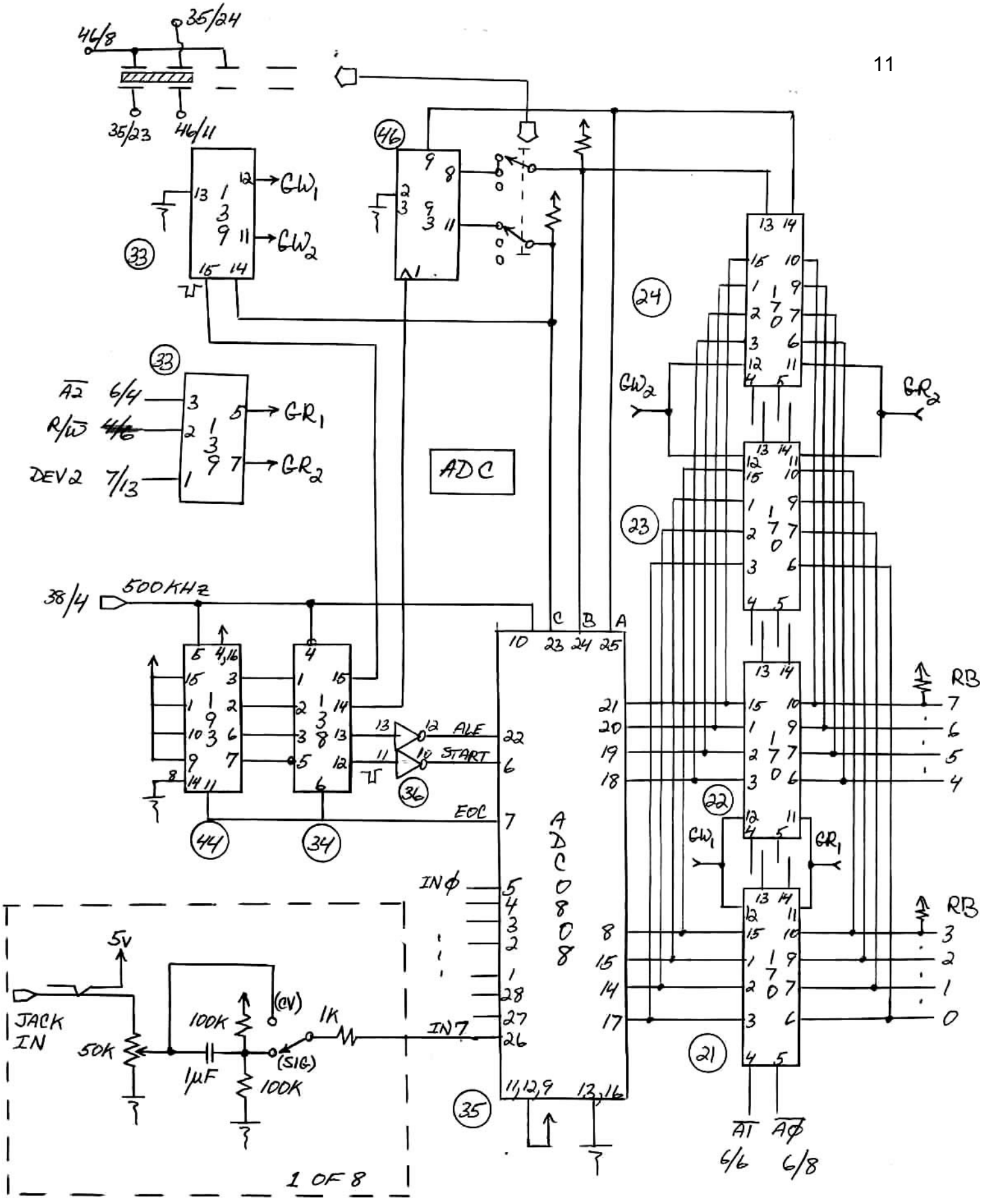
First, the number of the register to be loaded (0 - 15) must be written into micro address 32787 (8013 Hex). (Take care, the register numbers in the Manual are in octal form.)

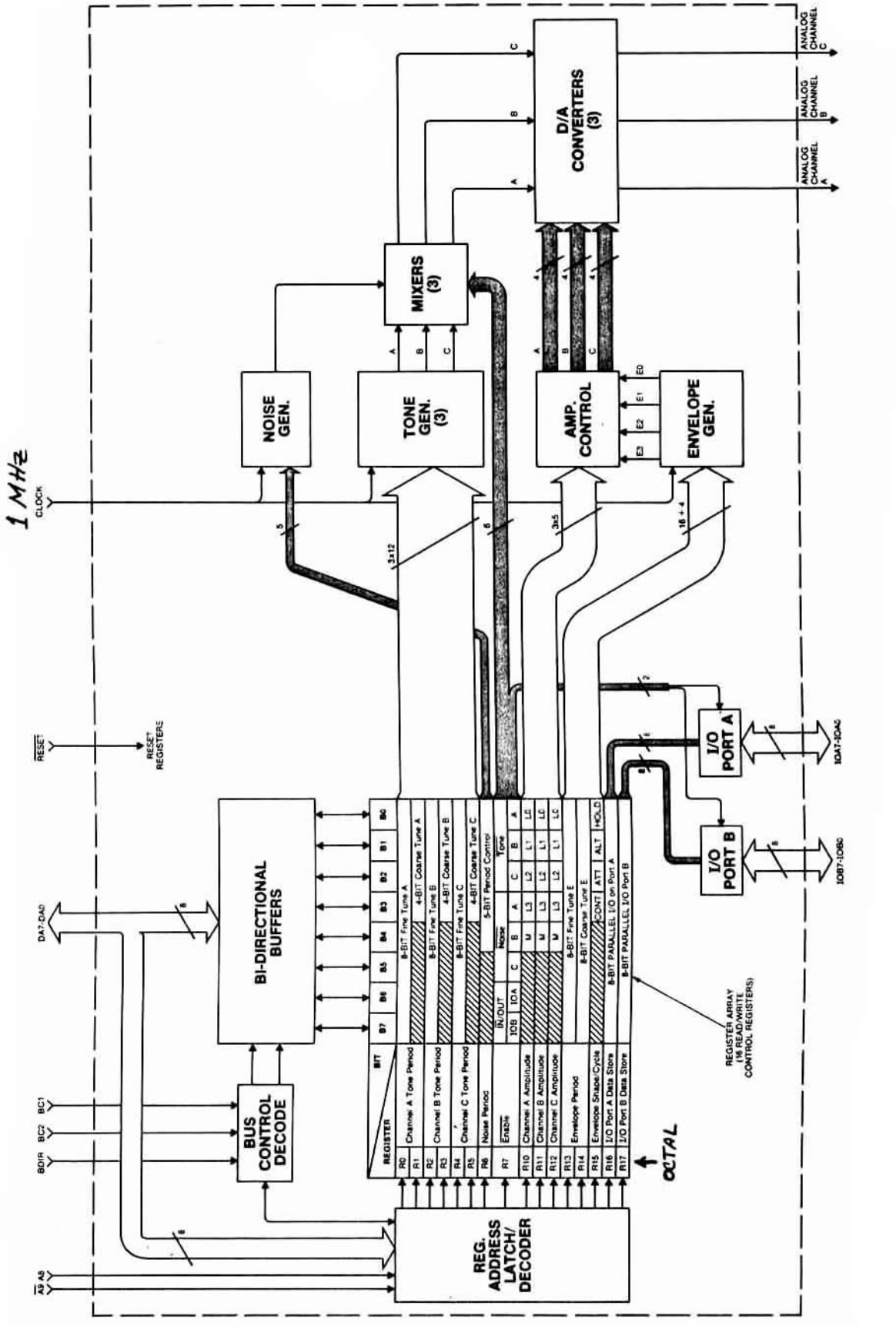
Second, the data to be loaded into the register must be written into micro address 32786 (8012 Hex). This step can be repeated any number of times until you want to change the register in which case you return to step one.

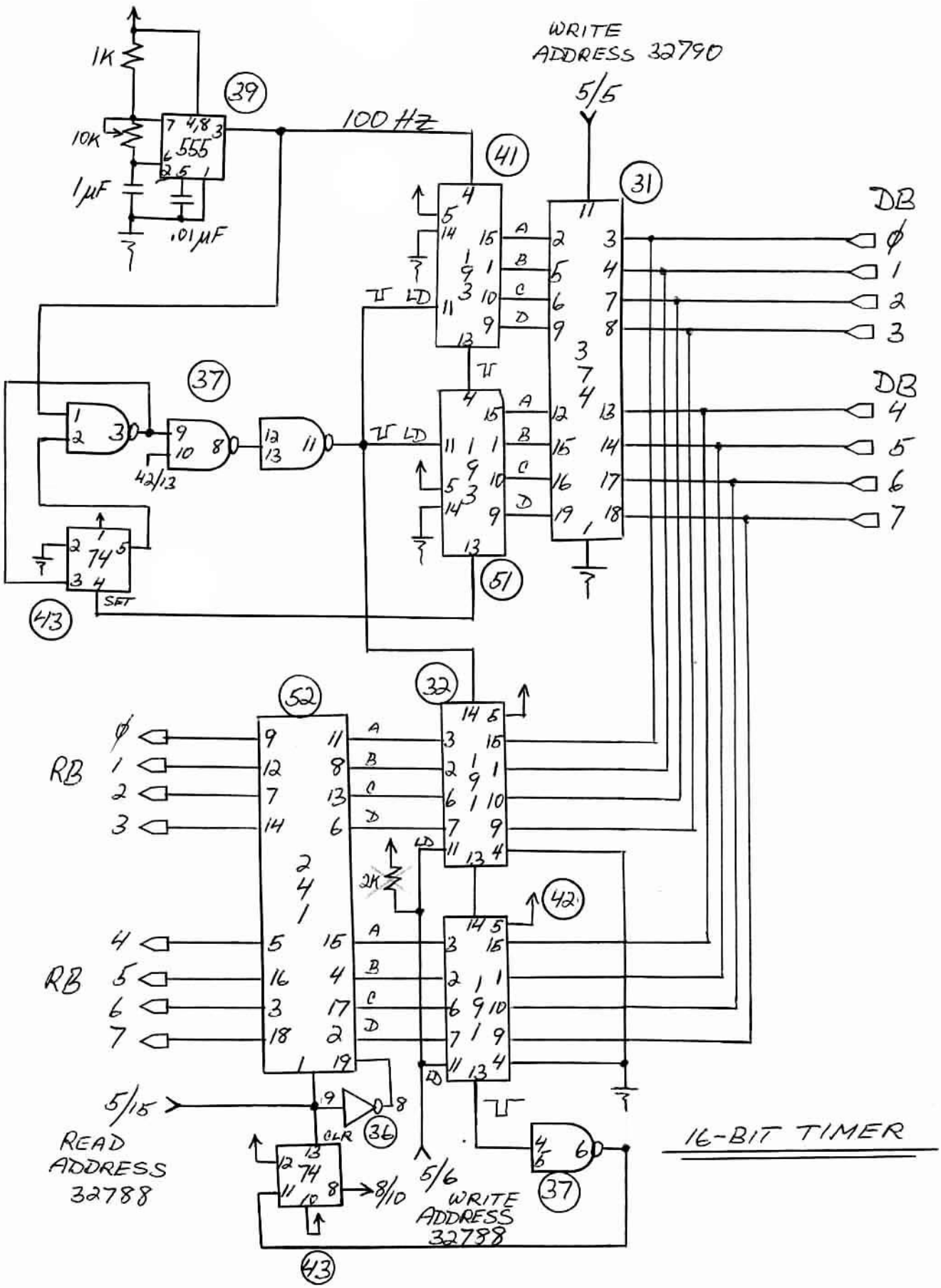

49
10K
.3 mA
0.1 µF
5/8
CLK
CLR
D0
1
2
3
4
5
0
1
2
3
4
5
1K
57
CLK
CLR
6
7
6
7
1K
47
55
SID
A
Y
3
1
8
9
1
2
4.7K
A
1K
4.7K
B
1K
4.7K
C
1K
1MHZ CLK
36
6/8
A0
5/7
PULSE GENERATOR
AY-SYNTHESIZER
8012_{16} LOAD DATA
8013_{16} LOAD REGISTER #

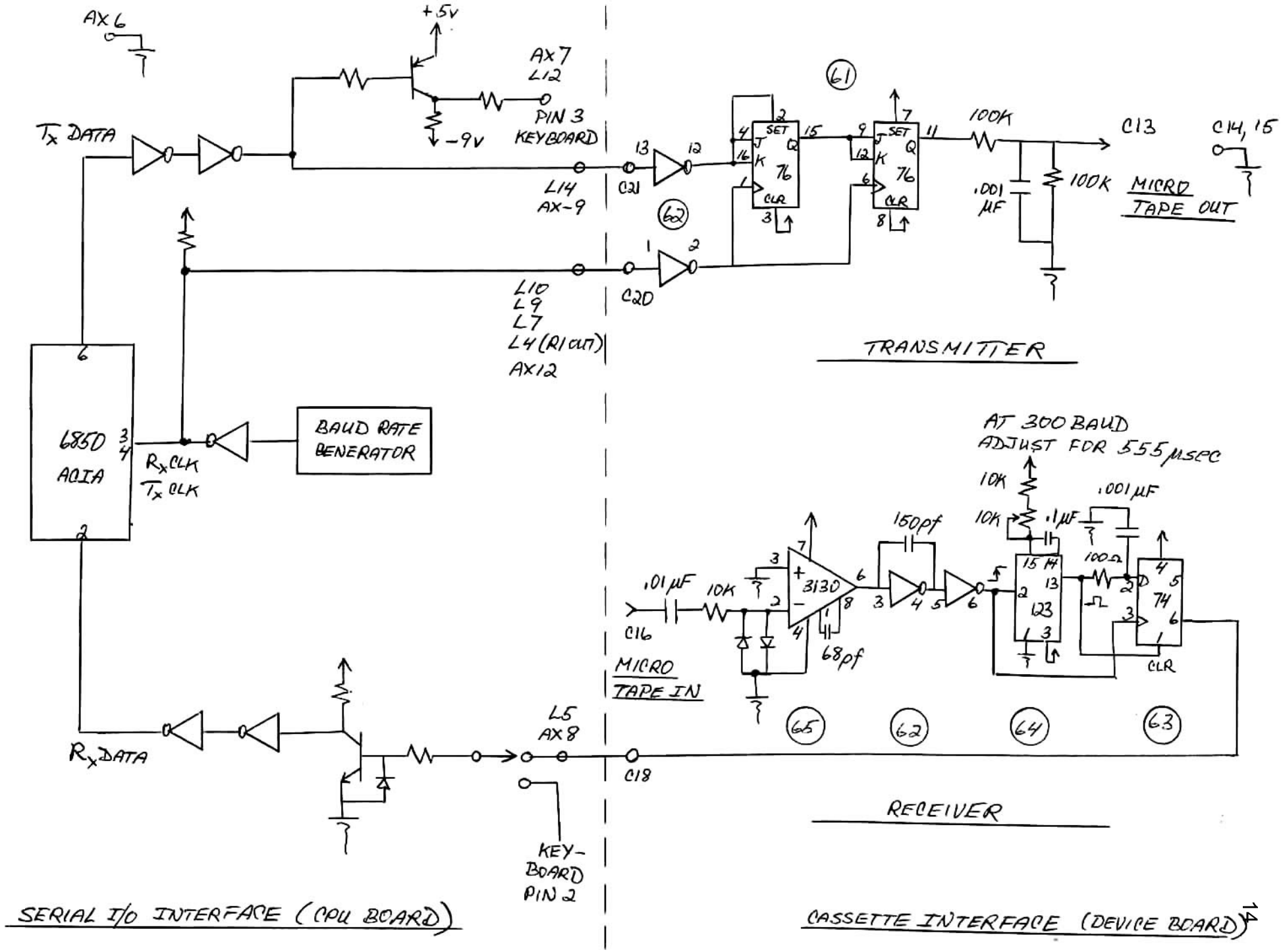

RESET
150K
100K
0
1
2
3
4
5
6
7
2900
NAND
54
69
67
53
49
SET
4.7K
0.1μF
8/9
6/8
5/17
RB7
PULSE DETECTOR


MULTIPLEXED DAC-8
2μS
CONVERT
SAMPLE 63/9
38/5
2MHz
393
74
SET
1408
318
324
139
DEV 2
R/W
.001μF
4.7μ
.1μ
5V
-9V
1K
2K
100Ω
10pf
100pf
470Ω
DB
W1
W2
A1
AØ


46/8
35/24
35/23
46/11
33
GW1
GW2
46
33
A2 6/4
R/W 4/6
DEV2 7/13
GR1
GR2
ADC
24
GW2
GR2
23
22
GW1
GR1
RB
21
AT 6/6
AØ 6/8
38/4
500KHZ
C B A
10 23 24 25
ALE
START
EOC
36
44
34
35
INØ
IN7
ADC0808
5V
JACK IN
50K
100K
(CV)
1K
(SIG)
1µF
100K
1 OF 8


1 MHz
CLOCK
NOISE GEN.
TONE GEN. (3)
MIXERS (3)
D/A CONVERTERS (3)
AMP. CONTROL
ENVELOPE GEN.
ANALOG CHANNEL A
ANALOG CHANNEL B
ANALOG CHANNEL C
RESET
RESET REGISTERS
BI-DIRECTIONAL BUFFERS
DA7-DA0
BUS CONTROL DECODE
BDIR
BC2
BC1
REG. ADDRESS LATCH/ DECODER
A9 A8
I/O PORT A
I/O PORT B
IOA7-IOA0
IOB7-IOB0
REGISTER ARRAY (16 READ/WRITE CONTROL REGISTERS)
OCTAL


1K
10K
1 µF
.01 µF
555
39
100 Hz
WRITE ADDRESS 32790
5/5
41
31
DB
LD
37
42/13
74
SET
43
51
52
32
RB
2K
42
36
CLR
5/15
READ ADDRESS 32788
8/10
5/6
WRITE ADDRESS 32788
16-BIT TIMER


AX 6
+5v
AX 7
L12
PIN 3
KEYBOARD
-9v
Tx DATA
L14
AX-9
C21
C20
61
62
100K
.001 µF
100K
C13
MICRO TAPE OUT
C14, 15
L10
L9
L7
L4 (RI OUT)
AX12
TRANSMITTER
6850 ACIA
RxCLK
Tx CLK
BAUD RATE GENERATOR
AT 300 BAUD
ADJUST FOR 555 µSEC
10K
.001 µF
10K
.1µF
150pf
.01 µF
10K
C16
MICRO TAPE IN
3130
68pf
100Ω
CLR
65
62
64
63
RxDATA
L5
AX 8
C18
KEY-BOARD PIN 2
RECEIVER
SERIAL I/O INTERFACE (CPU BOARD)
CASSETTE INTERFACE (DEVICE BOARD)