Euro Mega Controller

JT Feb 2017

The Euro Mega Controller is a programmable interface built in the Euro Rack format. All its devices are connected to an Arduino Mega 2560 microcontroller that can be programmed from any desktop computer through a USB connection using a readily available Programming Environment (IDE) software package. It can generate and read audio signals, pulse signals, analog synthesizer control voltages, and MIDI.

Here are some possible applications:

1. Programmed control or automation of an analog synthesizer using programmed Control Voltages and Pulse signals.

2. Generation of complex audio signals directly from the Arduino and controlled through its Control Voltage Inputs and pots.

3. Wavetable generation of signals using an 8-bit Digital to Analog Converter (DAC).

4. Simple signal processing of audio ADC inputs to a DAC audio output.

5. Generation of MIDI output signals to a synthesizer and controlled by the CV Inputs.

6. Manipulation of MIDI Input commands to be resent out the MIDI Ouput.

7. Modulation of external and internal pulse waveforms with a Diode Gate

8. Interfacing between Analog synthesizers and MIDI controlled synthesizers.

9. Input ports for sensors and switches programmed to generate MIDI commands or Analog Synthesizer control signals.

10. Exploration the audio capabilities of the Arduino Microprocessor.

Pulse Inputs

There are six pulse inputs designed to accept digital type signals. A LOW is zero volts and a HIGH is any voltage above about 2volts.

Input signals are received from either a mini-phone jack or a banana jack.

The signal received at the Arduino Digital Input is inverted from the jack inputs. A LOW becomes and HIGH, and a HIGH becomes a LOW. With no input signal, a HIGH appears at the Arduino input.

The Arduino digital inputs must be set up in the program to use internal pull-up resistors to complete the pulse input circuit.

Each Pulse Input includes a pushbutton which drives the Arduino input LOW when pressed.

Pulse Outputs

There are six Pulse Output circuits. These are digital outputs at zero or +5 volts. The Arduino can be programmed to put out static HIGHs or LOWs, Pulse waveform signals, or SquareWave signals.

The output appears on both a mini-phone jack and a banana jack. An LED indicator light shows the state of the output.

The actual output is inverted from the Arduino digital output pins. A LOW set on the Arduino digital output pin results in a HIGH on the Pulse Out jack and a dark LED indicator light. A HIGH set on the Arduino digital output pin results in a LOW on the Pulse Out jack and a lit LED indicator light.

Control Voltage Inputs

There are six CV Inputs. These inputs accept voltages from zero to +5 volts. Anything higher than +5 volts is clamped to 5v at the Arduino input.

The input circuit incorporates an Envelope Follower. Audio inputs will be converted to a control voltage that follows the amplitude of the input. Regular Control Voltage signals will pass through the Envelope Follower with only a small 0.3v drop in voltage.

This device will accept two inputs from the mini-phone and banana jacks. The combined input will be the higher of the two.

With no input attached to the miniphone jack, a 0 to 5v pot control takes over the input.

Control Voltage Outputs

There are six CV outputs. These are connected to Arduino digital output pins through a simple RC filter with a 72Hz cutoff frequency. The output is connected to both a mini-phone jack and a banana jack.

These outputs are designed to work with Arduino Pulse Width Modulated signals. The RC filter will filter out the frequency of the PWM signal (490Hz or 976Hz) and leave a control voltage that varies with the pulse width of the PWM signal. A 72Hz cutoff will allow for Low Frequency Oscillator (LFO) generation using the PWM.

MIDI Interface

The rightmost Euro module has MIDI Output and MIDI Input jacks. These are connected to a secondary set of serial I/O lines, the Serial1 pins of the Arduino Mega (Tx on pin 18 and Rx on pin 19). This allows for the Serial USB to be used exclusively for programming the Arduino.

It is recommended that you use the Arduino MIDI library to program the MIDI I/O. Setting it up requires just two program lines before the Setup() section:

```
#include <MIDI.h>
MIDI_CREAT_INSTANCE(HardwareSerial, Serial1, MIDI);
```

The first line loads the MIDI Library. Make sure you use version 4 or later. Check the online documentation for instruction on how to install the MIDI library into your Arduino IDE app.

The second line creates an Instance of the MIDI library Object to use in your Arduino program. “HardwareSerial” specifies that you are using actual pins dedicated to Serial I/O on the Mega, as opposed to a simulated software type of Serial I/O. “Serial1” directs the Object to use pins 18 and 19 on the Mega. Using “Serial” would direct it to use Pins 0 and 1, which are dedicated to the USB serial lines used to program the Mega. “MIDI” can be changed to any name you want, to refer to this MIDI Library Object in your own program.

Digital to Analog Converter (DAC)

Just above the MIDI is the output for an 8-bit DAC. The connection can be made with either a miniphone plug or a banana plug.

The DAC is an Analog Devices AD7224 chip. The 8 bits of data inputs are connected to pins A0 through A7 of the Mega, which can be accessed as PORTF. For example, to put the value 53 onto the A0-A7 lines use the command:

```
PORTF = 53;
```

To load this value into the DAC, momentarily pull the Write line of the chip low, which is on pin 37.

```
digitalWrite(37, LOW);
digitalWrite(37, HIGH);
```

Vref of the DAC is connected to the 3.3v line of the Arduino Mega. This means that a zero on inputs of the DAC will result in zero volts on the output, and 255 on the inputs will result in a 3.3volt output.

Diode Gate

Just above the DAC out is the 5-input Diode Gate. The Diode Gate is meant to be used with Digital signals, meaning Pulse or Squarewaves. Using other types of audio signals may or may not produce interesting results.

The gate used is actually an OR Gate. A HIGH on any of the inputs will clamp the output HIGH, thus a low subaudio frequency input will effectively gate the other inputs on and off. When all the inputs are in the audio range, the result is a complex modulated output that only goes LOW when all the inputs are LOW.

There are five inputs to the Diode Gate. Three of them miniphone jacks arranged around the Red Reset Button and two are internally connected to Arduino pins 38 and 39. Unused inputs should be either left unconnected or tied LOW. Directly below the input jacks is the one miniphone output jack for the Diode Gate.

The tone() function of the Arduino is useful for creating a squarewave audio signal to input to the Diode Gate. The only problem is that it can only be used on one Arduino output pin. Any additional signals must be programmed with delay() functions or complex Timer/Interrupt schemes.

Signal Processing Inputs

The two jacks on either side of the Red Reset button serve as inputs to the Diode Gate. They are also sent to the Analog Input pins A14 and A15 of the Arduino after being biased at 2.5 volts. The Arduino Analog to Digital Converters (ADC) only reads voltage

between 0 and +5 volts. Most audio signals sit at zero volts oscillating between both negative and positive voltages. Biasing a signal up above zero volts allows it to be read by the Arduino's ADC converters.

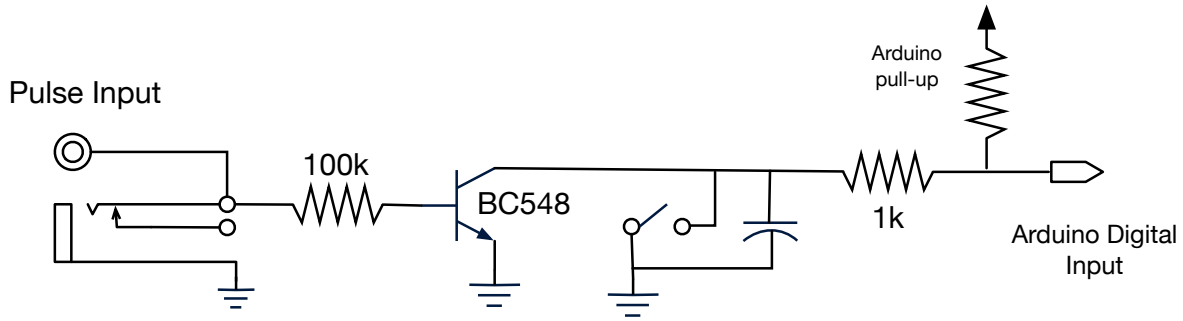
Arduino ADC converters along with the AD7224 DAC can be used for simple digital signal processing. The slow processor speed of the Arduino may limit the complexity of the program.

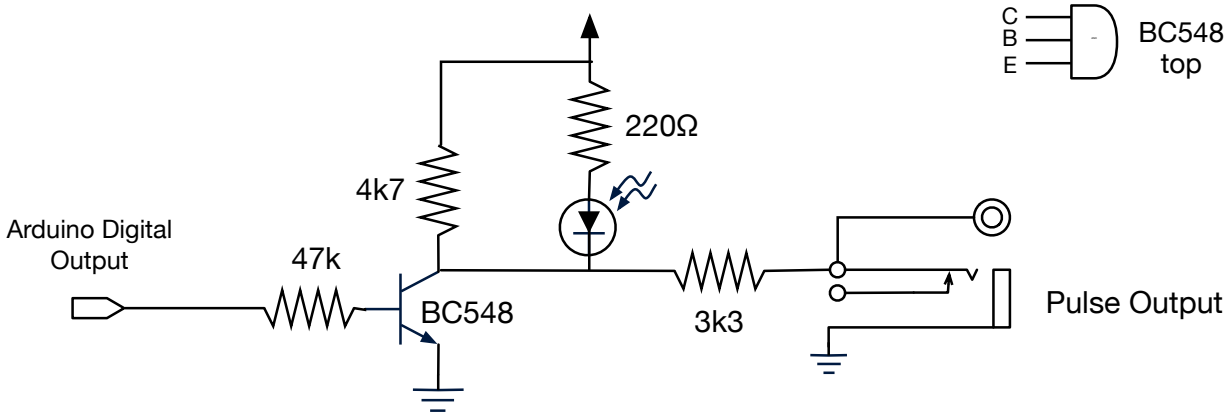
Euro UniBuffers

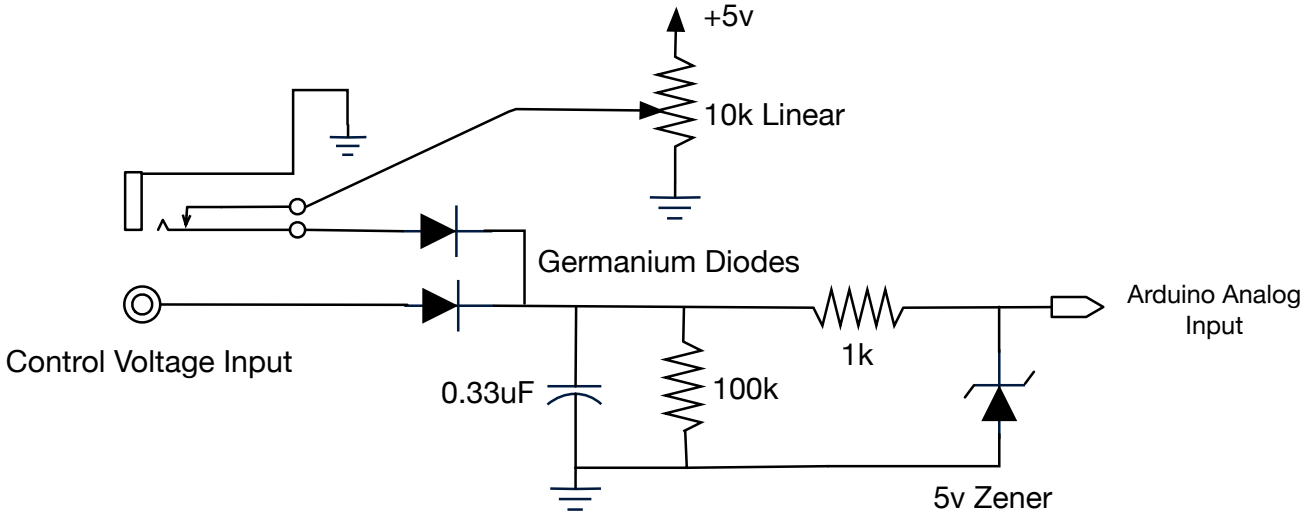
Two Simple Euro Buffer Modules have been added to the Euro Controller for signal routing convenience. A unity gain mixer combines up to four CV or Audio signals for a single summed output. A buffered mult provides up to four buffered outputs from a single CV or Audio input.

	Euro Mega Arduino Pin Connections JT 2/2017
0	Rx0 -- USB programming
1	Tx0 -- USB programming
2	**Pulse Input 1** (interrupt 4)
3	**Pulse Input 2** (interrupt 5)
4	CV Output 1 (PWM, timer0)
5	CV Output 2 (PWM, timer3)
6	CV Output 3 (PWM, timer4)
7	CV Output 4 (PWM, timer4)
8	CV Output 5 (PWM, timer4)
9	Pulse Output 1 *can't use tone() and PWM on pins 9 & 10 so made it PulseOut
10	Pulse Output 2
11	CV Output 6 (PWM, timer)
12	Pulse Output 3
13	Pulse Output 4
14	Pulse Output 5
15	Pulse Output 6
16	**Pulse Input 3**
17	**Pulse Input 4**
18	MIDI Out Tx, Serial1
19	MIDI In Rx, Serial1
20	**Pulse Input 5** (interrupt 0) SDA
21	**Pulse Input 6** (interrupt 1) SCL
37	DAC Write Pulse (active low)
38	Input to Diode Gate
39	Input to Diode Gate
A0-A7	Data Inputs to DAC AD7224 chip
A8-13	CV Inputs 1-6
A14	Signal Input biased up to 2.5v from Diode Gate Input Left
A15	Signal Input biased up to 2.5v from Diode Gate Input Right

Euro Mega Controller



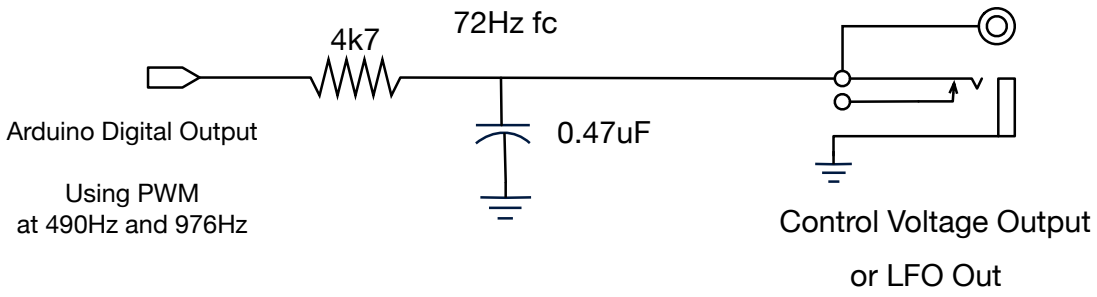


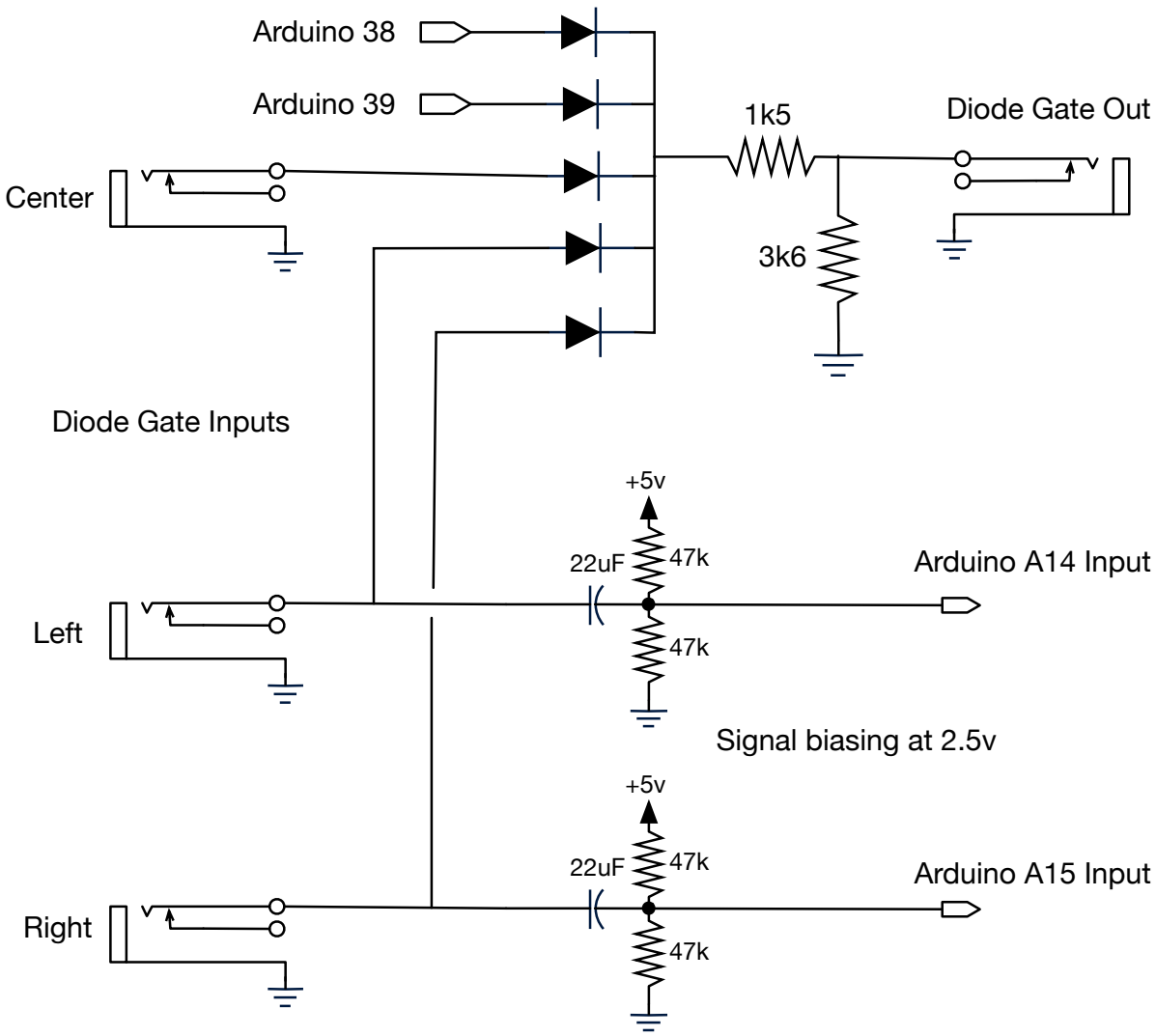


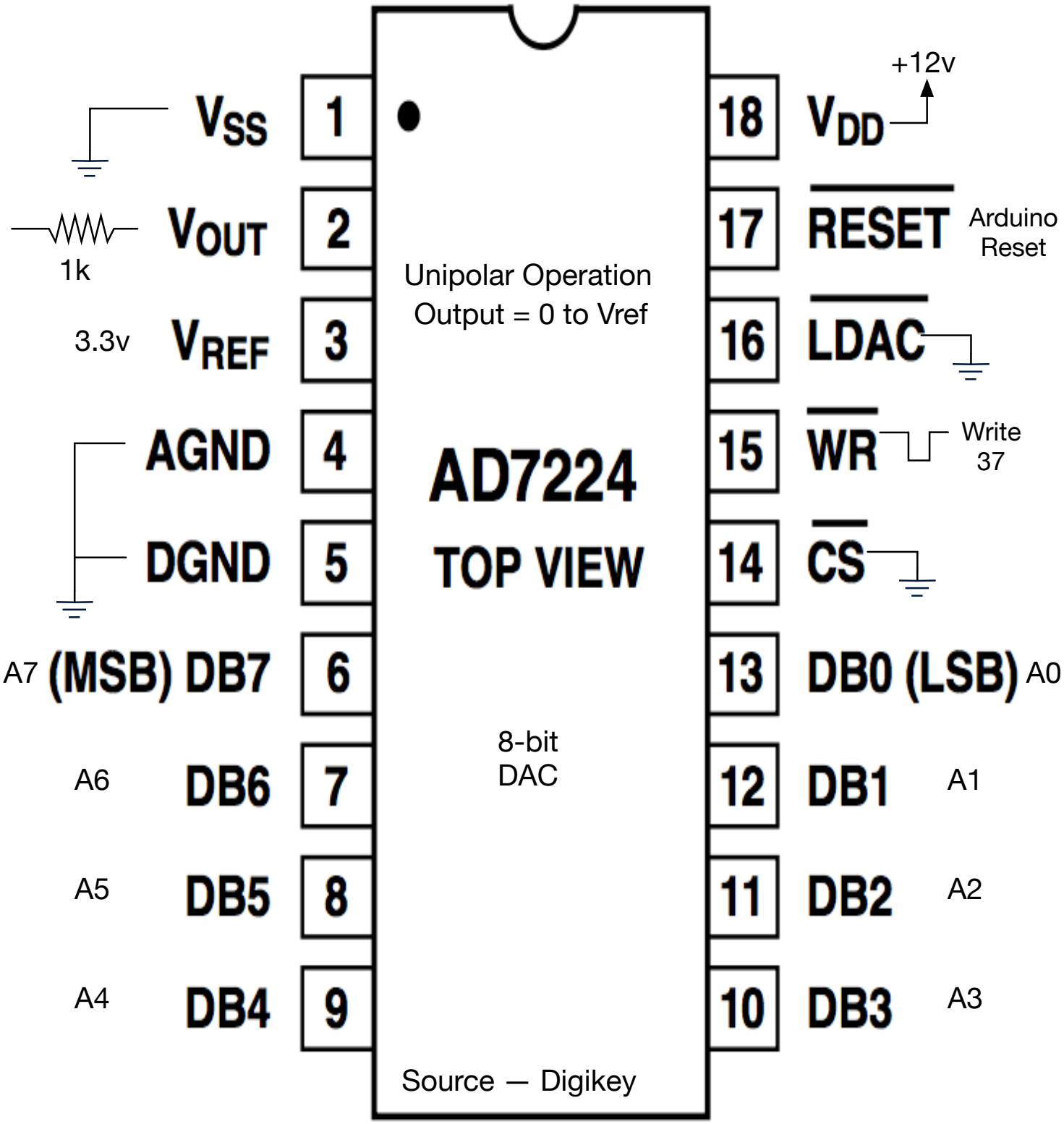
Envelope Follower

JT 2/2017

Euro Mega Controller






+12v
VSS
1
18
VDD
VOUT
2
17
RESET
Arduino Reset
1k
Unipolar Operation
Output = 0 to Vref
3.3v
VREF
3
16
LDAC
AGND
4
AD7224
15
WR
Write 37
DGND
5
TOP VIEW
14
CS
A7
(MSB) DB7
6
13
DB0 (LSB)
A0
8-bit DAC
A6
DB6
7
12
DB1
A1
A5
DB5
8
11
DB2
A2
A4
DB4
9
10
DB3
A3
Source — Digikey

Arduino Music and Audio Projects
Mike Cook

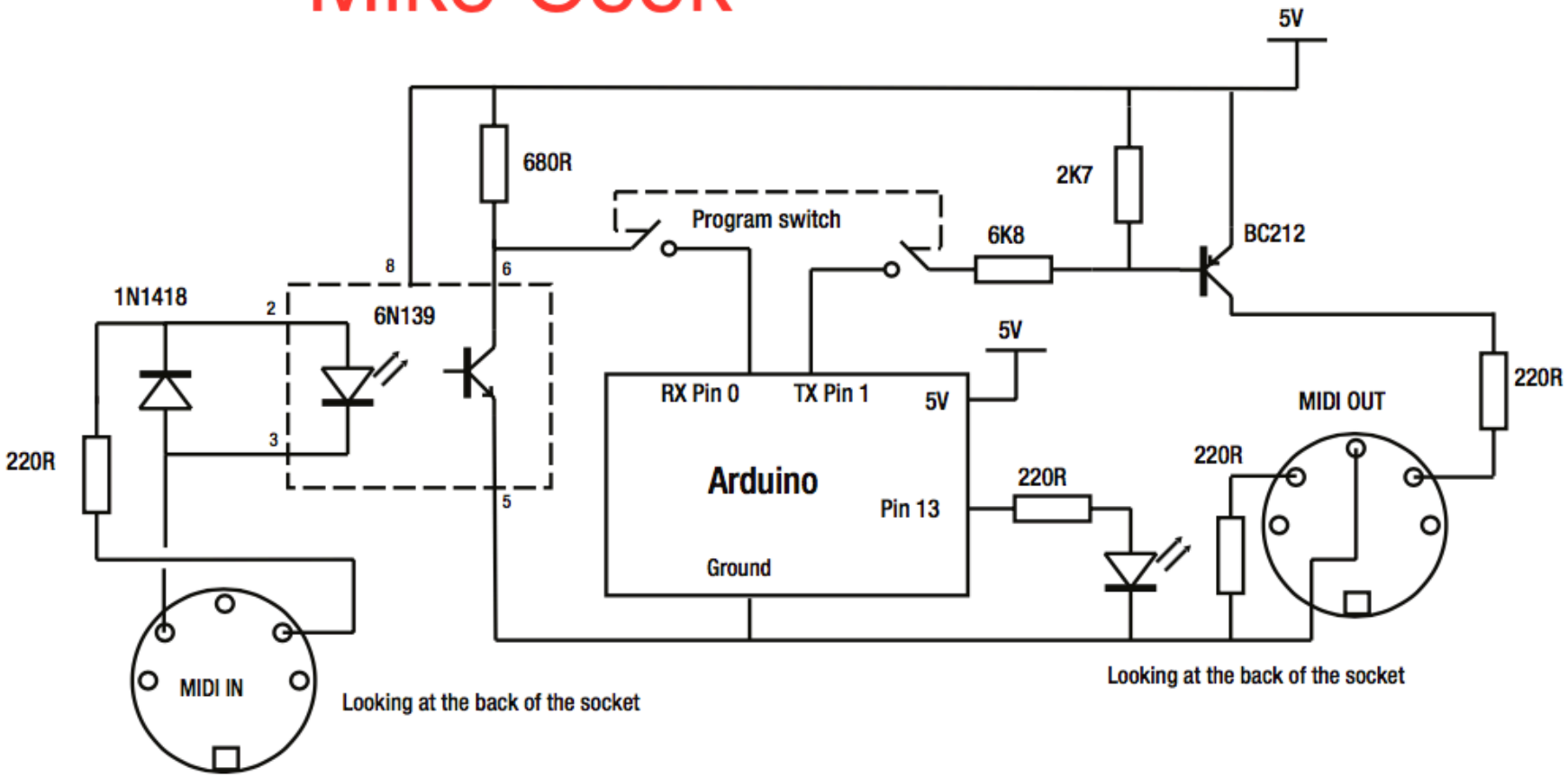
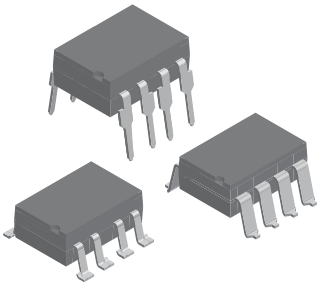
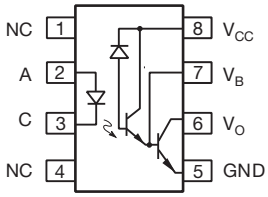


Figure 2-8. *Schematic of the MIDI shield*

High Speed Optocoupler, 100 kBd, Low Input Current, Photodiode Darlington Output





FEATURES

- High current transfer ratio, 300 %
- Low input current, 0.5 mA
- High output current, 60 mA
- Isolation test voltage, 5300 V_{RMS}
- TTL compatible output, V_{OL} = 0.1 V
- High common mode rejection, 500 V/µs
- Adjustable bandwidth-access to base
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e3

RoHS COMPLIANT

DESCRIPTION

High common mode transient immunity and very high current ratio together with 5300 V_{RMS} insulation are achieved by coupling and LED with an integrated high gain photo detector in an eight pin dual-in-line package. Separate pins for the photo diode and output stage enable TTL compatible saturation voltages with high speed operation.

Access to the base terminal allows adjustment to the gain bandwidth.

The 6N138 is ideal for TTL applications since the 300 % minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 kΩ pull-up resistor.

The 6N139 is best suited for low power logic applications involving CMOS and low power TTL. A 400 % current transfer ratio with only 0.5 mA of LED current is guaranteed from 0 °C to 70 °C.

Caution: Due to the small geometries of this device, it should be handled with Electrostatic Discharge (ESD) precautions. Proper grounding would prevent damage further and/or degradation which may be induced by ESD.

APPLICATIONS

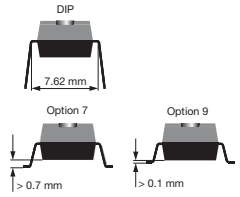
- Microprocessor system interface
- PLC, ATE input / output isolation
- EIA RS232 line receiver
- TTL, CMOS voltage level translation
- Multiplexed data transmission
- Digital control power supply
- Ground loop and electrical noise elimination

AGENCY APPROVALS

- UL1577, file no. E52744, double protection
- DIN EN 60747-5-5 available with option 1

ORDERING INFORMATION

6	N	1	3	#	-	X	0	#	#	T
PART NUMBER						PACKAGE OPTION				TAPE AND REEL



AGENCY CERTIFIED/PACKAGE	CTR (%)	
	1.6 mA	
UL	**> 300**	**> 500**
DIP-8	6N138	6N139, 6N139-X001
SMD-8, option 7	6N138-X007T	6N139-X007, 6N139-X007T
SMD-8, option 9	6N138-X009T	6N139-X009, 6N139-X009T
VDE	**> 300**	**> 500**
SMD-8, option 7	-	6N139-X017T
SMD-8, option 9	-	6N139-X019T

Note

- For additional information on the available options refer to option information.

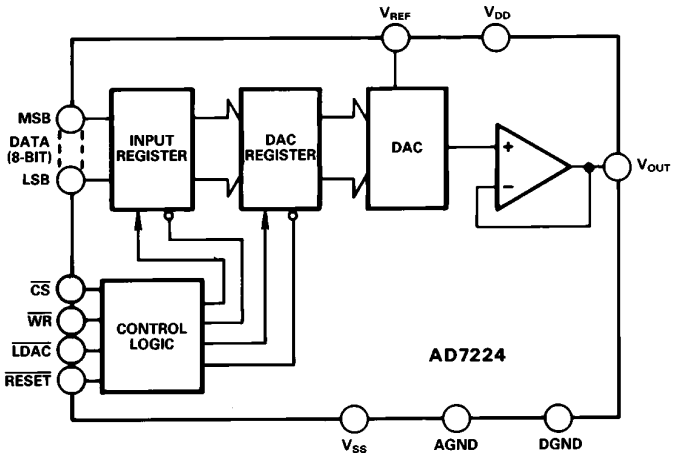
ANALOG DEVICES

LC²MOS 8-Bit DAC with Output Amplifiers

AD7224

FEATURES
8-Bit CMOS DAC with Output Amplifiers
Operates with Single or Dual Supplies
Low Total Unadjusted Error:
Less Than 1 LSB Over Temperature
Extended Temperature Range Operation
µP-Compatible with Double Buffered Inputs
Standard 18-Pin DIPs, and 20-Terminal Surface Mount Package and SOIC Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7224 is a precision 8-bit voltage-output, digital-to-analog converter, with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers–an input register and a DAC register. Only the data held in the DAC registers determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224s. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5 V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 V to +12.5 V when using dual supplies. The part is also specified for single supply operation using a reference of +10 V. The output amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35 mW typical with single supply).
2. Low Total Unadjusted Error
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC²MOS) process coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1 LSB over the full operating temperature range.
3. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7224 allows operation from a single power supply rail. The part can also be operated with dual supplies giving enhanced performance for some parameters.
4. Versatile Interface Logic
   The high speed logic allows direct interfacing to most microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7224 in multiple DAC systems. The part also features a zero override function.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD7224–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4 V to 16.5 V, V_{SS} = –5 V ± 10%; AGND = DGND = 0V; V_{REF} = +2 V to (V_{DD} – 4 V)[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15 V ± 5%, V_{REF} = +10 V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±3/2	±1	LSB max	
Full-Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14 V to 16.5 V, V_{REF} = +10 V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±50	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	V min to V max	
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1s.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]				
Positive Full-Scale Change	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Negative Full-Scale Change	7	7	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough	50	50	nV secs typ	V_{REF} = 0 V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V min/V max	For Specified Performance
V_{SS} Range	4.5/5.5	4.5/5.5	V min/V max	For Specified Performance
I_{DD}				
@ 25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{MIN} to T_{MAX}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}				
@ 25°C	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{MIN} to T_{MAX}	5	5	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]				
t_1				
@ 25°C	90	90	ns min	Chip Select/Load DAC Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_2				
@ 25°C	90	90	ns min	Write/Reset Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_3				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_4				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_5				
@ 25°C	90	90	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	ns min	
t_6				
@ 25°C	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: –40°C to +85°C
B, C Versions: –40°C to +85°C
T, U Versions: –55°C to +125°C
[3]Sample Tested at 25°C by Product Assurance to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.

Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +15 V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10 V[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1s.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2	2	V/μs min	
Voltage Output Settling Time[4]				
Positive Full-Scale Change	5	5	μs max	Settling Time to ±1/2 LSB
Negative Full-Scale Change	20	20	μs max	Settling Time to ±1/2 LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0 V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V min/V max	For Specified Performance
I_{DD}				
@ 25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{MIN} to T_{MAX}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3, 4]				
t_1				
@ 25°C	90	90	ns min	Chip Select/Load DAC Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_2				
@ 25°C	90	90	ns min	Write/Reset Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_3				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_4				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_5				
@ 25°C	90	90	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	ns min	
t_6				
@ 25°C	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7224KN, LN: 0°C to +70°C
AD7224BQ, CQ: –25°C to +85°C
AD7224TD, UD: –55°C to +125°C
[3]See Terminology.
[4]Sample tested at 25°C by Product Assurance to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND . . . . . –0.3 V, +17 V
V_{DD} to DGND . . . . . –0.3 V, +17 V
V_{DD} to V_{SS} . . . . . –0.3 V, +24 V
AGND to DGND . . . . . –0.3 V, V_{DD}
Digital Input Voltage to DGND . . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND . . . . . –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND[2] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above 75°C by . . . . . 6 mW/°C
Operating Temperature
Commercial (K, L Versions) . . . . . –40°C to +85°C
Industrial (B, C Versions) . . . . . –40°C to +85°C
Extended (T, U Versions) . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7224KN	–40°C to +85°C	±2 max	N-18
AD7224LN	–40°C to +85°C	±1 max	N-18
AD7224KP	–40°C to +85°C	±2 max	P-20A
AD7224LP	–40°C to +85°C	±1 max	P-20A
AD7224KR-1	–40°C to +85°C	±2 max	R-20
AD7224LR-1	–40°C to +85°C	±1 max	R-20
AD7224KR-18	–40°C to +85°C	±2 max	R-18
AD7224LR-18	–40°C to +85°C	±1 max	R-18
AD7224BQ	–40°C to +85°C	±2 max	Q-18
AD7224CQ	–40°C to +85°C	±1 max	Q-18
AD7224TQ	–55°C to +125°C	±2 max	Q-18
AD7224UQ	–55°C to +125°C	±1 max	Q-18
AD7224TE	–55°C to +125°C	±2 max	E-20A
AD7224UE	–55°C to +125°C	±1 max	E-20A

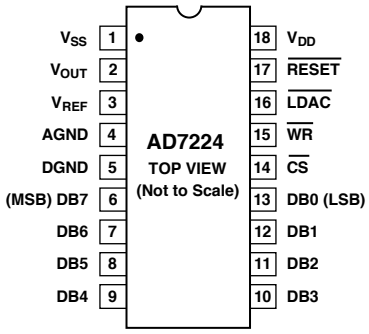
NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

CAUTION

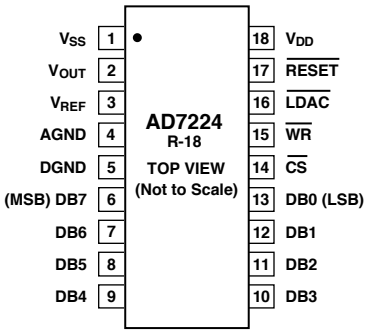
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7224 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

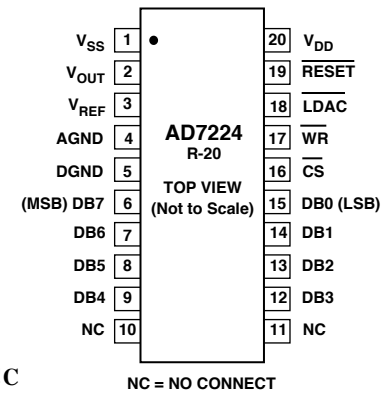
DIP and SOIC



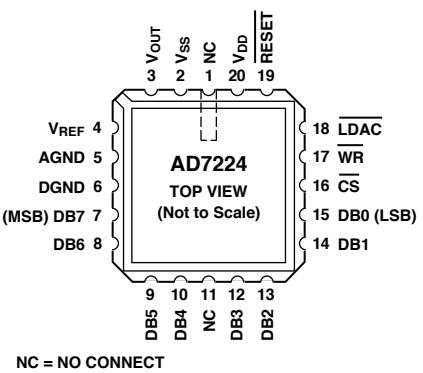
(SOIC)



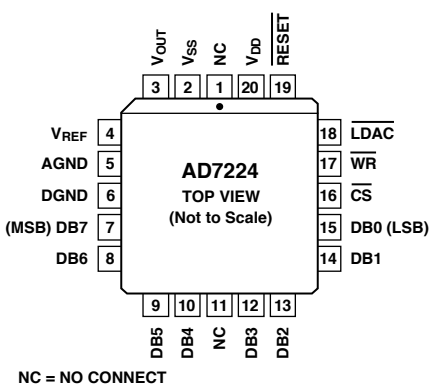
(SOIC)



LCCC



PLCC



TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full-scale error, relative accuracy and zero code error. Maximum output voltage is V_{REF} – 1 LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error, relative to the LSB size, will increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSBs over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10 V.

RELATIVE ACCURACY

Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for zero code error and full-scale error and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output due to a change in the digital input code. It is specified in nV secs and is measured at V_{REF} = 0 V.

FULL-SCALE ERROR

Full-Scale Error is defined as:

Measured Value – Zero Code Error – Ideal Value

CIRCUIT INFORMATION

D/A SECTION

The AD7224 contains an 8-bit voltage-mode digital-to-analog converter. The output voltage from the converter has the same polarity as the reference voltage, allowing single supply operation. A novel DAC switch pair arrangement on the AD7224 allows a reference voltage range from +2 V to +12.5 V.

The DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS single pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

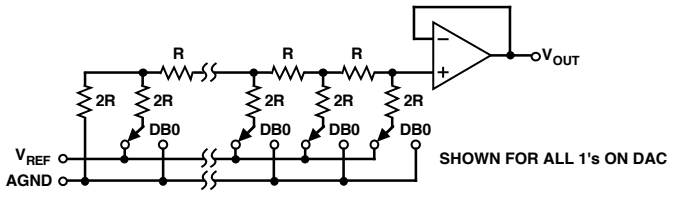


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin is code dependent and can vary from 8 kΩ minimum to infinity. The lowest input impedance occurs when the DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 25 pF to 50 pF.

The V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUT} = D \bullet V_{REF}$$

where D is a fractional representation of the digital input code and can vary from 0 to 255/256.

OP-AMP SECTION

The voltage-mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing +10 V across a 2 kΩ load and can drive capacitive loads of 3300 pF.

The AD7224 can be operated single or dual supply resulting in different performance in some parameters from the output amplifier. In single supply operation (V_{SS} = 0 V = AGND) the sink capability of the amplifier, which is normally 400 μA, is reduced as the output voltage nears AGND. The full sink capability of 400 μA is maintained over the full output voltage range by tying V_{SS} to –5 V. This is indicated in Figure 2.

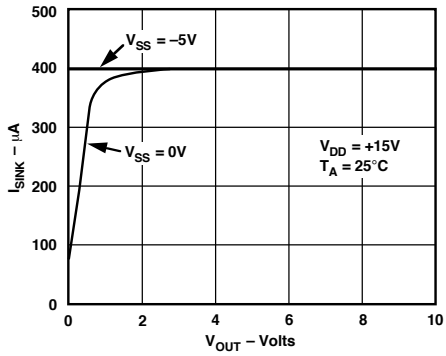


Figure 2. Variation of I_{SINK} with V_{OUT}

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

Additionally, the negative V_{SS} gives more headroom to the output amplifier which results in better zero code performance and improved slew-rate at the output, than can be obtained in the single supply mode.

DIGITAL SECTION

The AD7224 digital inputs are compatible with either TTL or 5 V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1 nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

Table I shows the truth table for AD7224 operation. The part contains two registers, an input register and a DAC register. $\overline{CS}$ and $\overline{WR}$ control the loading of the input register while $\overline{LDAC}$ and $\overline{WR}$ control the transfer of information from the input register to the DAC register. Only the data held in the DAC register will determine the analog output of the converter.

All control signals are level-triggered and therefore either or both registers may be made transparent; the input register by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC register by keeping $\overline{LDAC}$ and $\overline{WR}$ "LOW". Input data is latched on the rising edge of $\overline{WR}$.

Table I. AD7224 Truth Table

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↓	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↓	H	DAC Register Latched
L	X	X	X	Both Registers Loaded With All Zeros
↓	H	H	H	Both Register Latched With All Zeros and Output Remains at Zero
↓	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care.
All control inputs are level triggered.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line functions like a zero override with the output brought to 0 V for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on $\overline{RESET}$ will latch all 0s into the registers and the output remains at 0 V after the $\overline{RESET}$ line has returned "HIGH". The $\overline{RESET}$ line can be used to ensure power-up to 0 V on the AD7224 output and is also useful, when used as a zero override, in system calibration cycles. Figure 3 shows the input control logic for the AD7224.

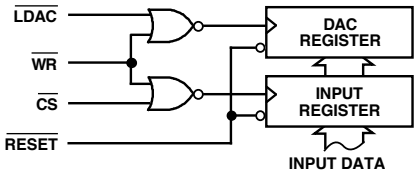
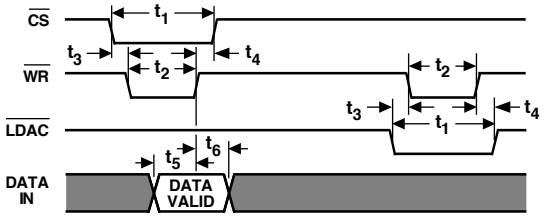


Figure 3. Input Control Logic



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. $t_r = t_f$ = 20ns OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$

Figure 4. Write Cycle Timing Diagram

SPECIFICATION RANGES

For the DAC to maintain specified accuracy, the reference voltage must be at least 4 V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

With dual supply operation, the AD7224 has an extended V_{DD} range from +12 V ± 5% to +15 V ± 10% (i.e., from +11.4 V to +16.5 V). Operation is also specified for a single V_{DD} power supply of +15 V ± 5%.

Performance is specified over a wide range of reference voltages from 2 V to (V_{DD} – 4 V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5 V bandgap reference and the AD584, a precision +10 V reference. Note that in order to achieve an output voltage range of 0 V to +10 V, a nominal +15 V ± 5% power supply voltage is required by the AD7224.

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7224. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7224 AGND and DGND pins (IN914 or equivalent).

Applying the AD7224

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7224, with the output voltage having the same positive polarity as V_{REF}. The AD7224 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 5. The voltage at V_{REF} must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

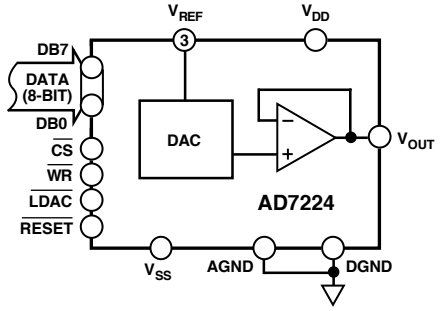


Figure 5. Unipolar Output Circuit

Table III. Unipolar Code Table

DAC Register Contents MSB	LSB	Analog Output
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0 V

Note: $1\ LSB = \left(V_{REF}\right)\left(2^{-8}\right) = V_{REF}\left(\frac{1}{256}\right)$

BIPOLAR OUTPUT OPERATION

The AD7224 can be configured to provide bipolar output operation using one external amplifier and two resistors. Figure 6 shows a circuit used to implement offset binary coding. In this case

$$V_O = \left(1 + \frac{R2}{R1}\right) \bullet \left(D \ V_{REF}\right) - \left(\frac{R2}{R1}\right) \bullet \left(V_{REF}\right)$$

With $R1 = R2$

$$V_O = (2\ D - 1) \bullet V_{REF}$$

where D is a fractional representation of the digital word in the DAC register.

Mismatch between R1 and R2 causes gain and offset errors; therefore, these resistors must match and track over temperature. Once again, the AD7224 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 6 with R1 = R2.

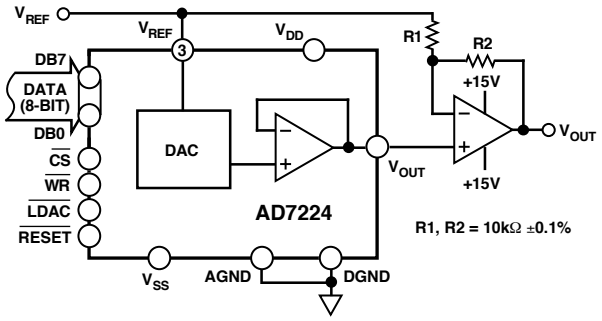


Figure 6. Bipolar Output Circuit

Table III. Bipolar (Offset Binary) Code Table

DAC Register Contents MSB	LSB	Analog Output
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	$0\ V$
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

AGND BIAS

The AD7224 AGND pin can be biased above system GND (AD7224 DGND) to provide an offset "zero" analog output voltage level. Figure 7 shows a circuit configuration to achieve this. The output voltage, V_{OUT}, is expressed as:

$$V_{OUT} = V_{BIAS} + D \bullet (V_{IN})$$

where D is a fractional representation of the digital word in DAC register and can vary from 0 to 255/256.

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4 V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

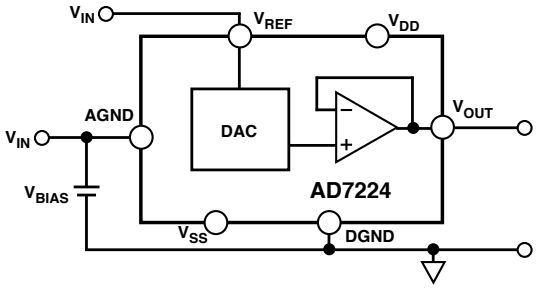


Figure 7. AGND Bias Circuit

MICROPROCESSOR INTERFACE

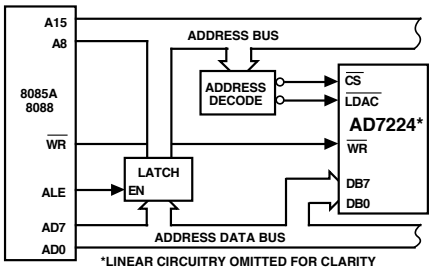


Figure 8. AD7224 to 8085A/8088 Interface

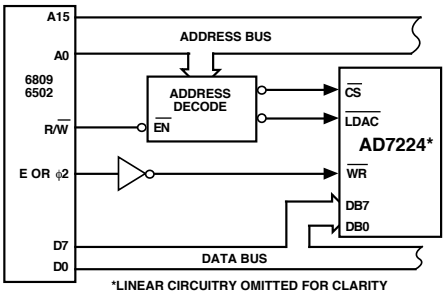


Figure 9. AD7224 to 6809/6502 Interface

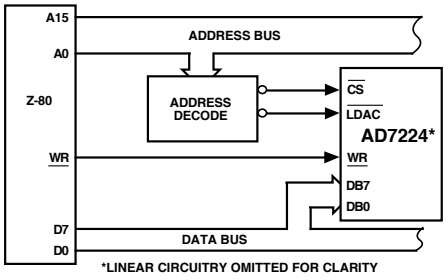


Figure 10. AD7224 to Z-80 Interface

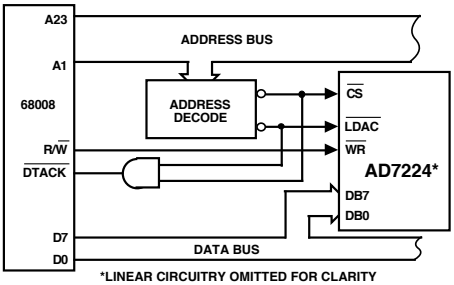


Figure 11. AD7224 to 68008 Interface

Arduino™ MEGA 2560