FEBRUARY 1979

AY-3-8910 AY-3-8912

Programmable Sound Generator

FEATURES

- ☐ Full software control of sound generation.
- ☐ Interfaces to most 8-bit and 16-bit microprocessors.
- ☐ Three independently programmed analog outputs.
- ☐ Two 8-bit general purpose I/O ports (AY-3-8910).
- ☐ One 8-bit general purpose I/O port (AY-3-8912).
- ☐ Single +5 Volt Supply.

DESCRIPTION

The AY-3-8910/8912 Programmable Sound Generator (PSG) is a Large Scale Integrated Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912 is manufactured in GI's N-Channel Ion Implant Process. Operation requires a single 5V power supply, a TTL compatible clock, and a microprocessor controller such as the GI 16-bit CP1600/1610 or one of GI's PIC 1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package; the AY-3-8912 has one port and 28 leads.

PIN FUNCTIONS

DA7--DA0 (input/output/high impedance): pins 30--37 (AY-3-8910)
Data/Address 7--0: pins 21--28 (AY-3-8912)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7--DA0 correspond to Register Array bits B7--B0. In the address mode, DA3--DA0 select the register # ($0--17_8$) and DA7--DA4 in conjunction with address inputs $\overline{A9}$ and A8 form the high order address (chip select).

A8 (input): pin 25 (AY-3-8910)
pin 17 (AY-3-8912)

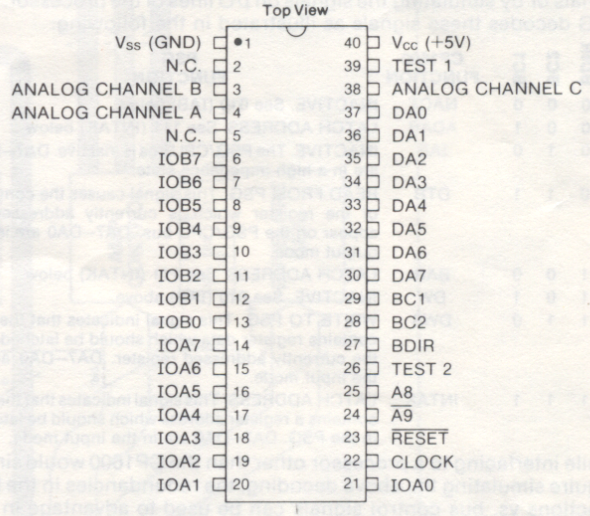
$\overline{A9}$ (input): pin 24 (AY-3-8910)
(not provided on AY-3-8912)

Address 9, Address 8

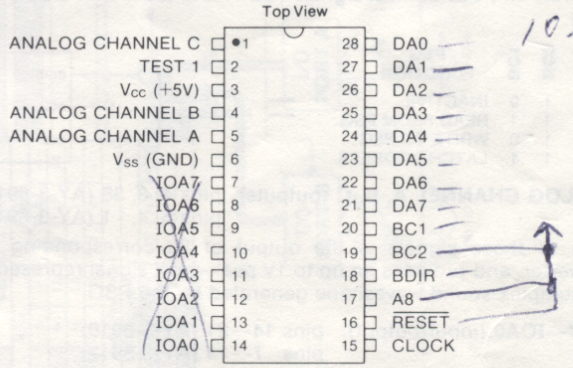
These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down ($\overline{A9}$) or pull-up (A8) resistor. In "noisy" environments, however, it is recommended that $\overline{A9}$ and A8 be tied to an external ground and +5V, respectively, if they are not to be used.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE
AY-3-8910



28 LEAD DUAL IN LINE
AY-3-8912



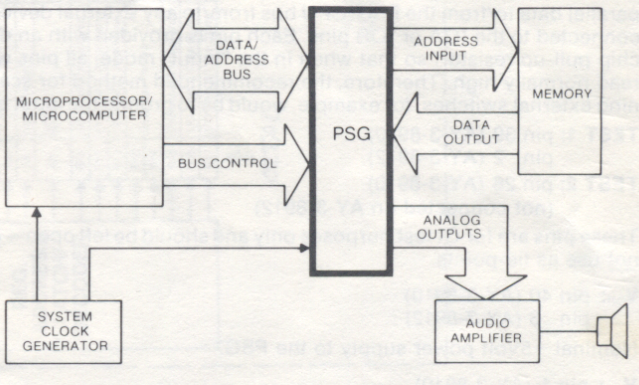


Fig. 1 SYSTEM BLOCK DIAGRAM

RESET (input): pin 23 (AY-3-8910)
pin 16 (AY-3-8912)

For initialization/power-on purposes, applying a logic "0" (ground) to the Reset pin will reset all registers to "0". The Reset pin is provided with an on-chip pull-up resistor.

CLOCK (input): pin 22 (AY-3-8910)
pin 15 (AY-3-8912)

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

BDIR, BC2, BC1 (inputs): pins 27,28,29 (AY-3-8910)
pins 18,19,20 (AY-3-8912)

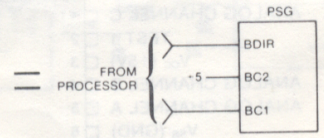
Bus DIRection, Bus Control 2,1

These bus control signals are generated directly by GI's CP1600 series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the CP1600, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor. The PSG decodes these signals as illustrated in the following:

BDIR	BC2	BC1	CP1600 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE. See 010 (IAB) below.
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK) below.
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive. DA7--DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7--DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK) below.
1	0	1	DW	INACTIVE. See 010 (IAB) above.
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7--DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode.

While interfacing to a processor other than the CP1600 would simply require simulating the above decoding, the redundancies in the PSG functions vs. bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V):

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS.



ANALOG CHANNEL A, B, C (outputs): pins 4, 3, 38 (AY-3-8910)
pins 5, 4, 1 (AY-3-8912)

Each of these signals is the output of its corresponding D/A Converter, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOA0 (input/output): pins 14--21 (AY-3-8910)
pins 7--14 (AY-3-8912)

IOB7--IOB0 (input/output): pins 6--13 (AY-3-8910)
(not provided on AY-3-8912)

Input/Output A7--A0, B7--B0

Each of these two parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high. Therefore, the recommended method for scanning external switches, for example, would be to ground the input bit.

TEST 1: pin 39 (AY-3-8910)
pin 2 (AY-3-8912)

TEST 2: pin 26 (AY-3-8910)
(not connected on AY-3-8912)

These pins are for GI test purposes only and should be left open—do not use as tie-points.

V_{CC}: pin 40 (AY-3-8910)
pin 3 (AY-3-8912)

Nominal +5Volt power supply to the PSG.

V_{SS}: pin 1 (AY-3-8910)
pin 6 (AY-3-8912)

Ground reference for the PSG.

ARCHITECTURE

The AY-3-8910/8912 is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through its 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits A8 and $\overline{A9}$) are decoded as follows:

* $\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0

THRU

0	1	0	0	0	0	1	1	1	1

HIGH ORDER (Chip Select) — LOW ORDER (Register #)

* $\overline{A9}$ is not provided on the AY-3-8912.

The four low order address bits select one of the 16 registers (R0--$R17_8$). The six high order address bits function as "chip selects" to control the tri-state bidirectional buffers (when the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$ A8 are fixed in the PSG design to recognize a 01 code; high order address bits DA7--DA4 may be mask-programmed to any 4-bit code by a special order factory mask modification. Unless otherwise specified, address bits DA7--DA4 are programmed to recognize only a 0000 code. A valid high order address latches the register address (the low order 4 bits) in the Register Address Latch/Decoder block. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (inactive, latch address, write data, or read data) is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	produce the basic square wave tone frequencies for each channel (A,B,C)
Noise Generator	produces a frequency modulated pseudo random pulse width square wave output.
Mixers	combine the outputs of the Tone Generators and the Noise Generator. One for each channel (A,B,C).
Amplitude Control	provides the D/A Converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator.
Envelope Generator	produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
D/A Converters	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control.

I/O PORTS

Two additional blocks are shown in the PSG Block Diagram which have nothing directly to do with the production of sound—these are the two I/O Ports (A and B). Since virtually all uses of microprocessor-based sound would require interfacing between the outside world and the processor, this facility has been included in the PSG. Data to/from the CPU bus may be read/written to either of two 8-bit I/O Ports without affecting any other function of the PSG. The I/O Ports are TTL-compatible and are provided with internal pull-ups on each pin. Both Ports are available on the AY-3-8910; only I/O Port A is available on the AY-3-8912.

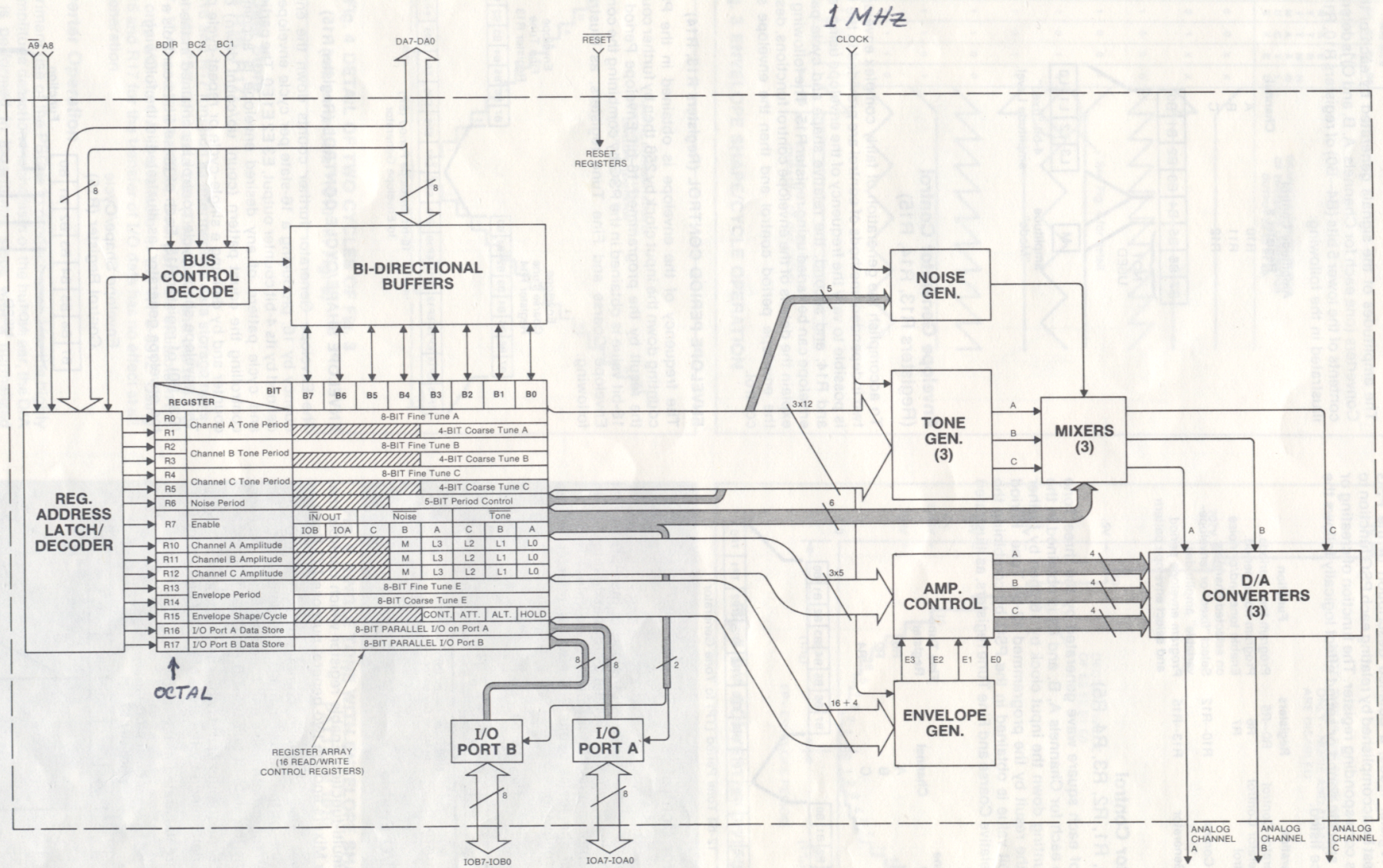


Fig. 2 PSG BLOCK DIAGRAM

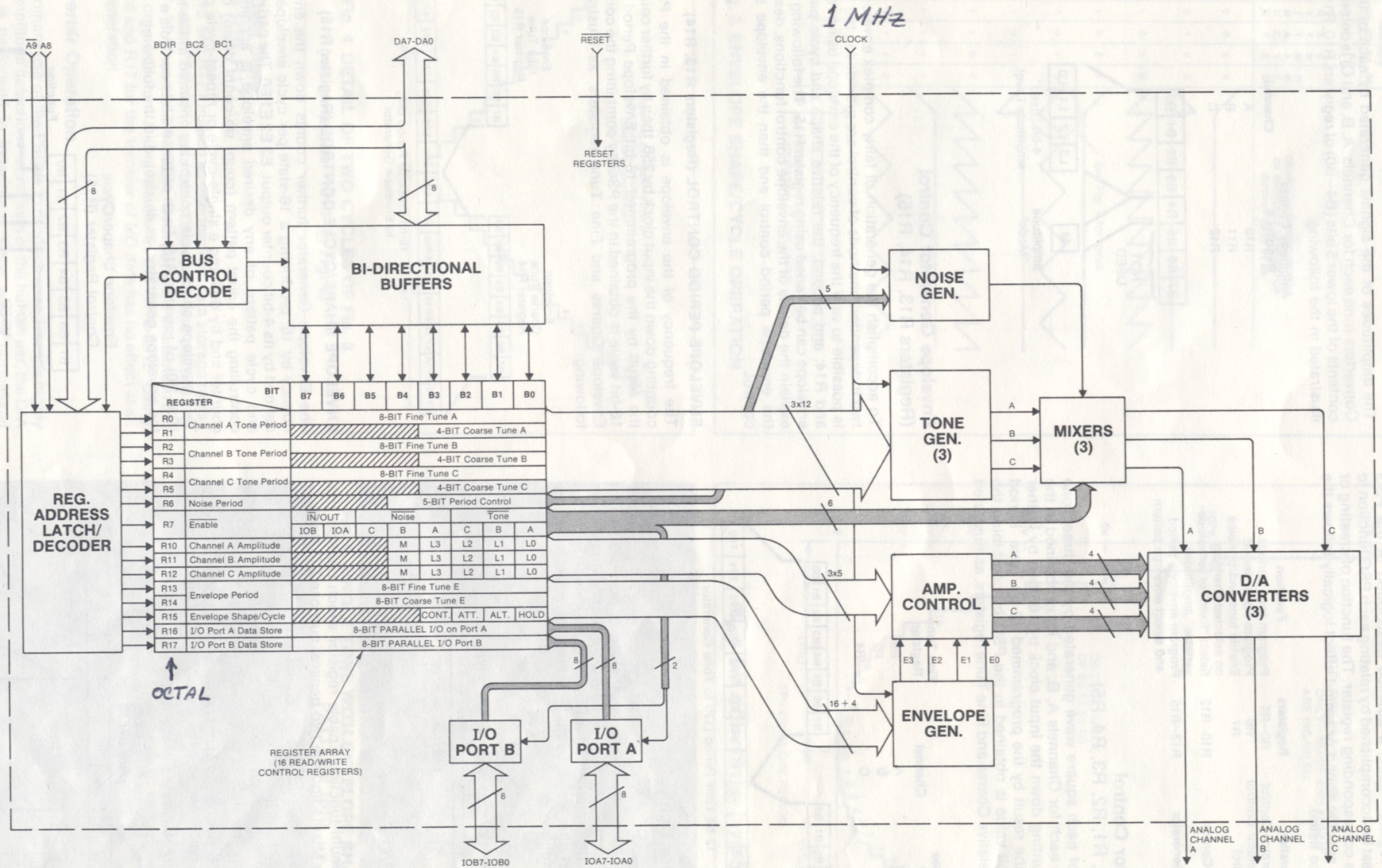


Fig. 2 PSG BLOCK DIAGRAM

OPERATION

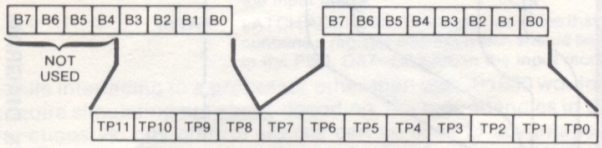
Since all functions of the PSG are controlled by the host processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers	Function
Tone Generator Control	R0--R5	Program tone periods.
Noise Generator Control	R6	Program noise period.
Mixer Control	R7	Enable tone and/or noise on selected channels.
Amplitude Control	R10--R12	Select "fixed" or "envelope-variable" amplitudes.
Envelope Generator Control	R13--R15	Program envelope period and select envelope pattern

Tone Generator Control
(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12-bit Tone Period value. Each 12-bit value is obtained in the PSG by combining the contents of the relative Coarse and Fine Tune registers, as illustrated in the following:

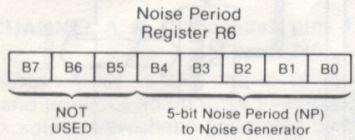
Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4



12-bit Tone Period (TP) to Tone Generator

Noise Generator Control
(Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5-bit Noise Period value. This 5-bit value consists of the lower 5 bits (B4--B0) of register R6, as illustrated in the following:



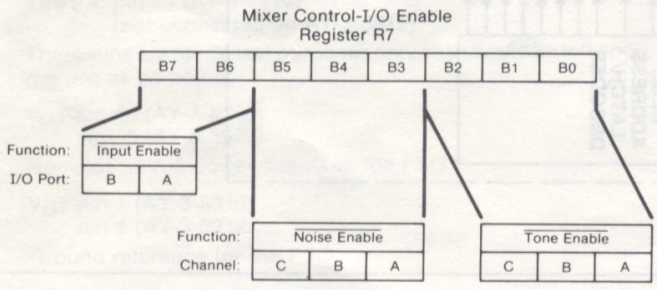
Mixer Control-I/O Enable
(Register R7)

Register 7 is a multi-function $\overline{\text{Enable}}$ register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports.

The Mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5--B0 of R7.

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

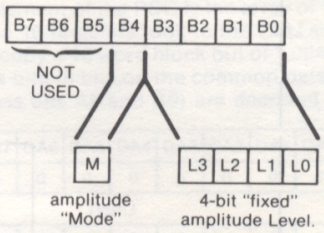
These functions are illustrated in the following:



Amplitude Control
(Registers R10, R11, R12)

The amplitudes of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the contents of the lower 5 bits (B4--B0) of registers R10, R11, and R12 as illustrated in the following:

Amplitude Control Register #	Channel
R10	A
R11	B
R12	C

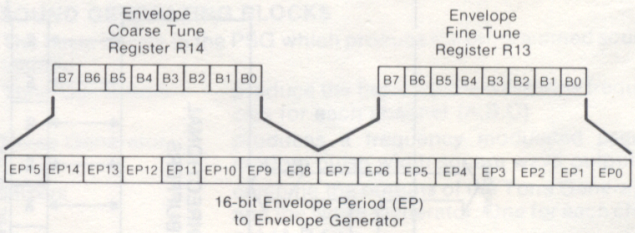


Envelope Generator Control
(Registers R13, R14, R15)

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG: first, it is possible to vary the frequency of the envelope using registers R13 and R14; and second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control.

ENVELOPE PERIOD CONTROL (Registers R13, R14)

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated in the following:

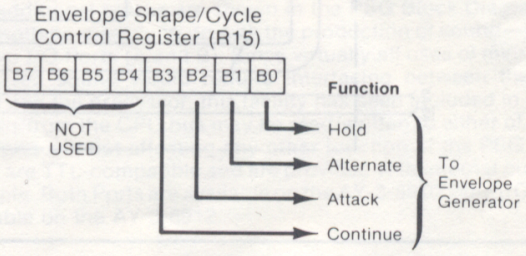


16-bit Envelope Period (EP) to Envelope Generator

ENVELOPE SHAPE/CYCLE CONTROL (Register R15)

The Envelope Generator further counts down the envelope frequency by 16, producing a 16-state per cycle envelope pattern as defined by its 4-bit counter output, E3 E2 E1 E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/count down) of the 4-bit counter and by defining a single-cycle or repeat-cycle pattern.

This envelope shape/cycle control is contained in the lower 4 bits (B3--B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following:



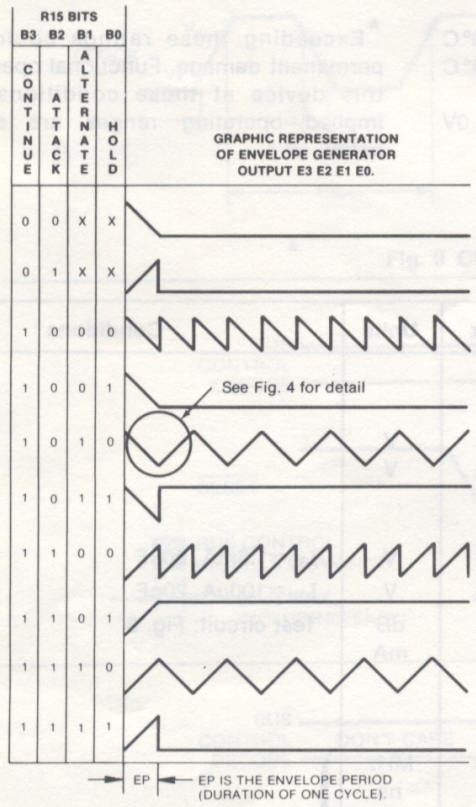


Fig. 3 ENVELOPE SHAPE/CYCLE OPERATION

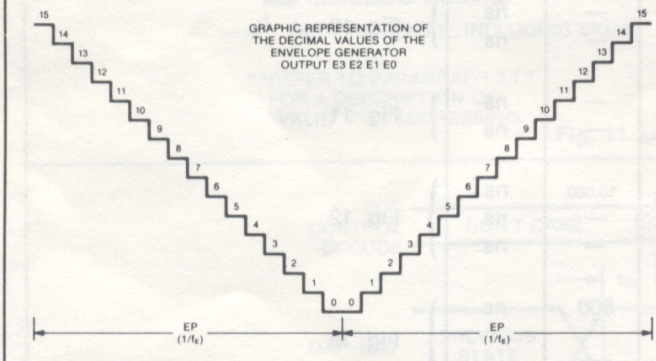


Fig. 4 DETAIL OF TWO CYCLES OF Fig. 3 (ref. waveform "1010" in Fig. 3)

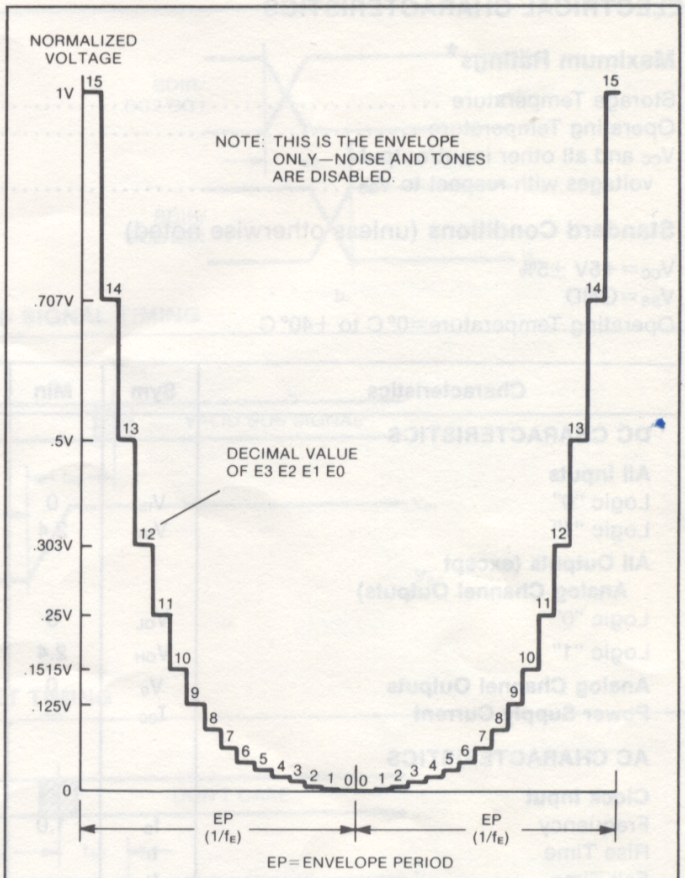


Fig. 5 D/A CONVERTER OUTPUT

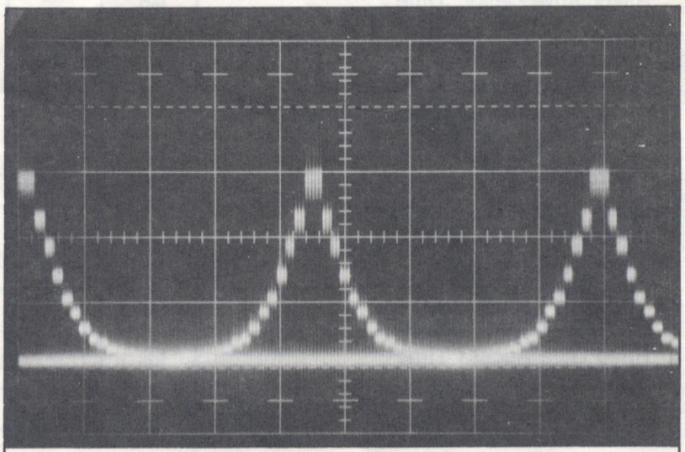


Fig. 6 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

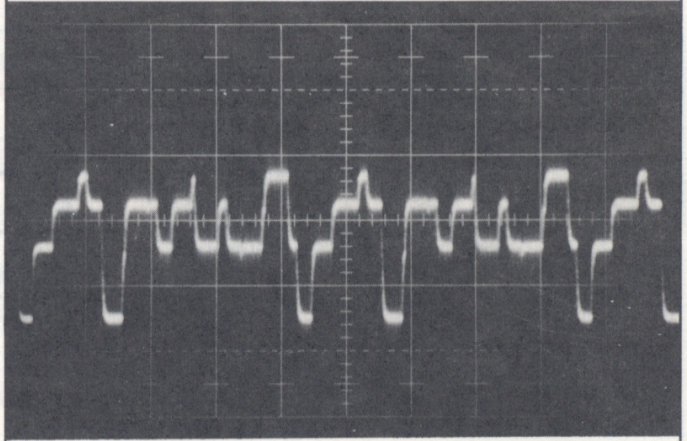


Fig. 7 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

I/O Port Data Store
(Registers R16, R17)

Registers R16 and R17 function as intermediate data storage registers between the PSG/CPU data bus (DA0--DA7) and the two I/O ports (IOA7--IOA0 and IOB7--IOB0). Both ports are available in the AY-3-8910; only I/O Port A is available in the AY-3-8912. Using registers R16 and R17 for the transfer of I/O data has no effect at all on sound generation.

D/A Converter Operation

Since the primary use of the PSG is to produce sound for the highly imperfect amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range of from 0 to 1 Volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4-bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other input/output voltages with respect to V_{SS} ..... −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +40°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
All Inputs						
Logic "0"	V_{IL}	0	—	0.6	V	
Logic "1"	V_{IH}	2.4	—	V_{CC}	V	
All Outputs (except Analog Channel Outputs)						
Logic "0"	V_{OL}	0	—	0.5	V	I_{OL} = 1.6mA, 20pF
Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA, 20pF
Analog Channel Outputs	V_O	0	—	60	dB	Test circuit: Fig. 8
Power Supply Current	I_{CC}	—	45	75	mA	
AC CHARACTERISTICS						
Clock Input						
Frequency	f_C	1.0	—	2.0	MHz	Fig. 9
Rise Time	t_r	—	—	50	ns	Fig. 9
Fall Time	t_f	—	—	50	ns	Fig. 9
Duty Cycle	—	25	50	75	%	Fig. 9
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{BD}	—	—	50	ns	Fig. 9
Reset						
Reset Pulse Width	t_{RW}	500	—	—	ns	Fig. 10
Reset to Bus Control Delay Time	t_{RB}	100	—	—	ns	Fig. 10
A9, A8, DA7--DA0 (Address Mode)						
Address Setup Time	t_{AS}	400	—	—	ns	Fig. 11
Address Hold Time	t_{AH}	100	—	—	ns	Fig. 11
DA7--DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	—	10,000	ns	Fig. 12
Write Data Setup Time	t_{DS}	50	—	—	ns	Fig. 12
Write Data Hold Time	t_{DH}	100	—	—	ns	Fig. 12
DA7--DA0 (Read Mode)						
Read Data Access Time	t_{DA}	—	250	500	ns	Fig. 13
DA7--DA0 (Inactive Mode)						
Tristate Delay Time	t_{TS}	—	100	200	ns	Fig. 13

**Typical values are at +25°C and nominal voltages.

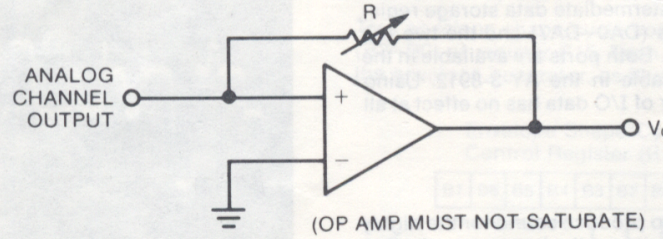


Fig. 8 ANALOG CHANNEL OUTPUT TEST CIRCUIT

TIMING DIAGRAMS

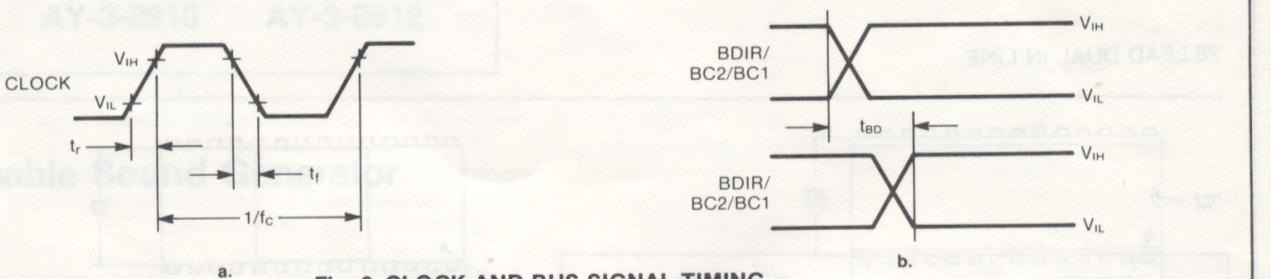


Fig. 9 CLOCK AND BUS SIGNAL TIMING

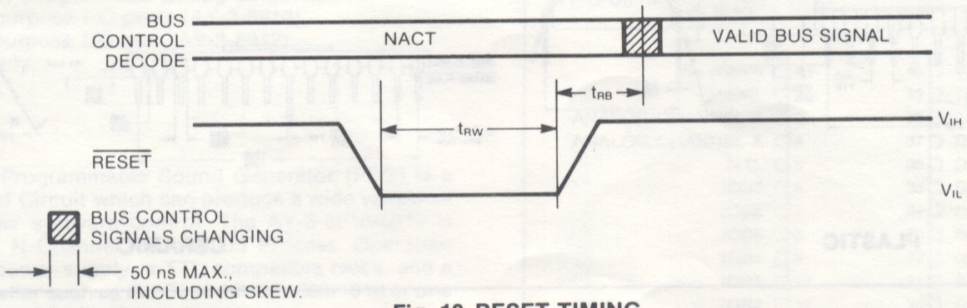
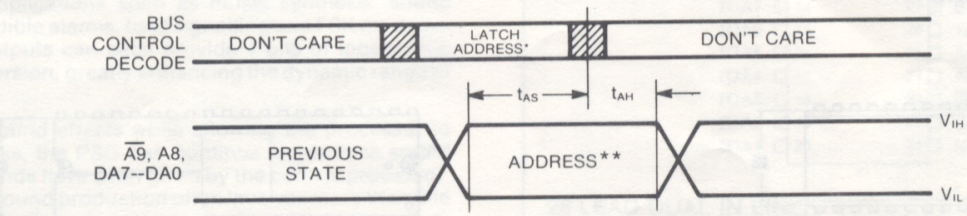


Fig. 10 RESET TIMING

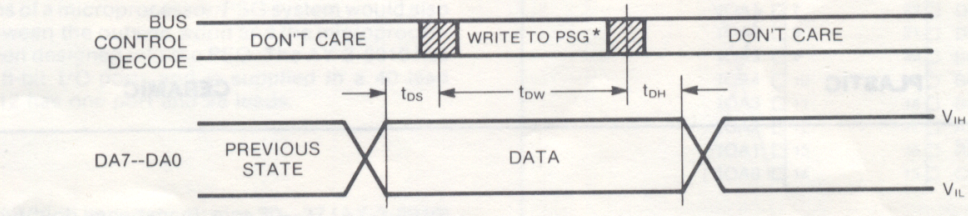


**REFER TO PARAGRAPH 2.1.1 FOR A DESCRIPTION OF "VALID" PSG ADDRESSING.

*ANY COMBINATION OF BDIR, BC2, BC1 WHICH DECODE "LATCH ADDRESS":

BDIR	BC2	BC1
0	0	1
or 1	0	0
or 1	1	1

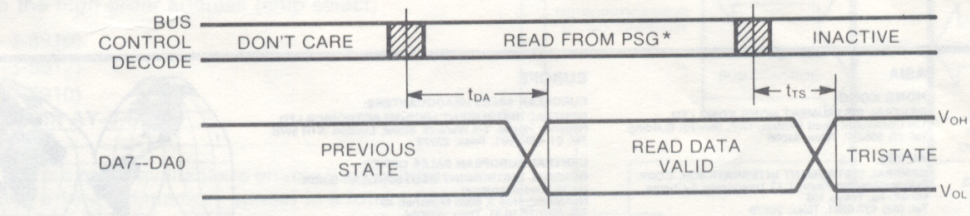
Fig. 11 LATCH ADDRESS TIMING



*"WRITE TO PSG":

BDIR	BC2	BC1
1	1	0

Fig. 12 WRITE DATA TIMING



*"READ FROM PSG":

BDIR	BC2	BC1
0	1	1

Fig. 13 READ DATA TIMING

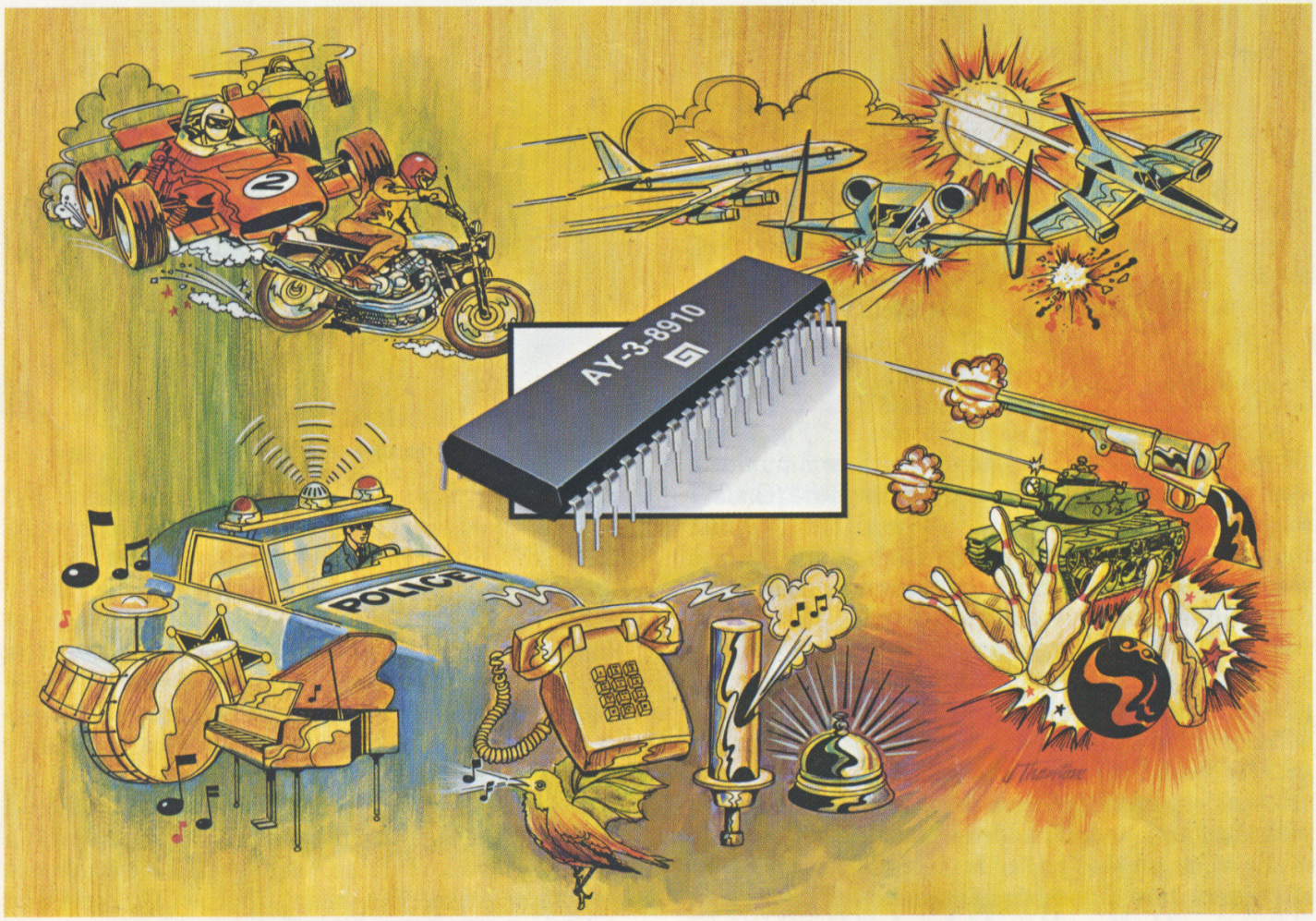
Software-controlled sound IC gives 'command performance'

Music and microprocessors usually don't mix—too much valuable time is wasted when a μP has to produce the music or sound effects for electronic games and musical instruments. But turn the job over to an LSI programmable sound generator, and you'll get software-produced sounds without constant attention from the processor.

Steven Burstein, Senior MOS Design Engineer, **Tom Mariner,** Software Consultant, and **John Wunner,** Group Director, Communications, General Instrument Corp., Microelectronics, 600 West John St., Hicksville, NY 11802.

You do it by letting μP commands direct the sound-creating circuits of a General Instrument AY-3-8910/8912 programmable sound generator (PSG), shown in Fig. 1. Not only can the IC play complete songs and generate complex sounds totally under software control, it can also sustain sound while the processor goes off to refresh, scan and service other system peripherals. What's more, the N-channel, ion-implant chip interfaces easily to any bus-oriented system. All you'll need to operate the PSG are a single 5-V supply, a TTL-compatible clock and either an 8 or 16-bit μP controller.

Since the PSG is controlled entirely by digital



1. **Sound effects, music, noise**—virtually no sound is beyond the capability of General Instrument's programmable sound generator ICs, the AY-3-8910 and 8912. Under microprocessor control, the devices generate sounds entirely from digital input commands. And microprocessor servicing of the chips is minimal.

GIMINI Cricket

The chip that chirps...

or cheeps, bleeps, hums, peeps, buzzes, dings, rings, roars, beeps, toots, blips, bongs, honks, hoots, hics, pings, booms, whistles, tats, or...

The point is, if you need a sound, GI's new "GIMINI Cricket" programmable sound generator, the AY-3-8910, can produce it. This gives a designer practically unlimited possibilities because, under full software control, the chip can generate complex sounds or combinations of sounds — music to soothe, rings and buzzes to alarm, and just about anything in between.

The AY-3-8910 is a natural for any products using microprocessors, interfacing easily to most 8- and 16-bit MPU's. In addition, it readily connects to most single-chip microcomputers — our PIC series, for example. The low-cost, AY-3-8910 has three independently programmed sound channels, an analog envelope generator, and two general purpose 8-bit I/O ports.

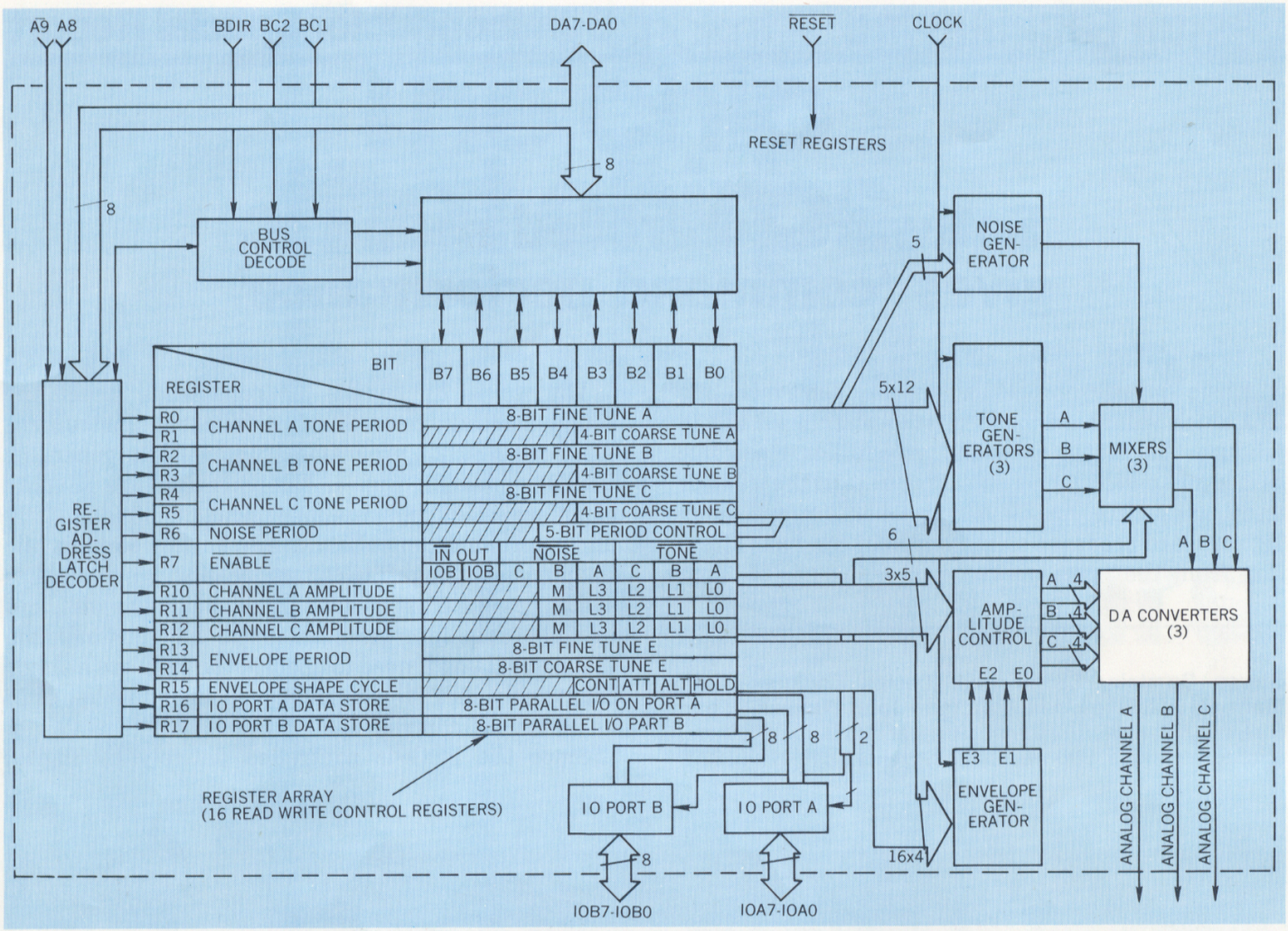
And all that's required for operation is a single 5V supply, a 2 MHz clock and a microprocessor controller.

With virtually all the hardware necessary to meet most audio needs, the AY-3-8910 has immediate application for a wide variety of systems and products providing audible signals, synthesized music and unique sound effects, to name but a few. The "GIMINI Cricket" chip is available in quantity and ready to chirp, cheep, beep — or whatever you decide to program into your product.

For more information on the AY-3-8910 and a free copy of our 1978 Product Guide, write to General Instrument Microelectronics, 600 West John Street, Hicksville, New York 11802, or call (516) 733-3379.

We help you compete.

GENERAL INSTRUMENT CORPORATION
MICROELECTRONICS



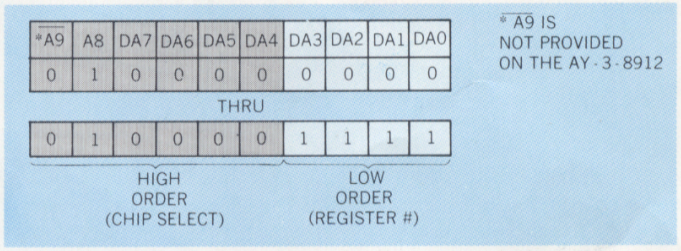
2. **Sixteen memory-mapped registers, designated R_0 through R_{17}, direct operations** inside the PSG. Once programmed, sounds are generated and sustained without further processor intervention. At the output, three independently programmed analog channels can create realistic sound effects or music.

commands, it generates a wide variety of sounds without any changes to its external circuitry. And chances are good that just a single device can create all the music or sound that your system will ever need.

Architecturally sound

At the heart of the PSG's architecture (Fig. 2) are 16 read/write-control registers, which communicate with a processor through a memory-mapped I/O. CPU commands are written into the 16 registers to direct the sound generator's operation. Each register is also readable, so the processor can determine its stored data value at any time.

To a CPU, the 16 registers (R_0 through R_{17} in Fig. 2) appear as a 16-word block of memory out of a possible 1024 address locations. Each register has ten address bits—8 bits come in on the common data/address bus, while two other bits (A_8 and $\overline{A_9}$) are sent separately. Addresses are decoded on-chip, with the four low-order address bits used to select one of the 16 registers (Fig. 3). The six high-order bits are chip-select lines that control the on-board, three-state bidirectional buffers. If the high-order bits contain an incorrect code, the buffers are forced into their high-impedance states.



3. **It takes ten bits to address** one of the PSG's 16 registers. The four low-order bits select one of the registers; the six high-order bits are chip select lines.

Bits A_8 and $\overline{A_9}$ are fixed in the PSG architecture —only code 01 is recognized. High-order address bits DA_4 through DA_7 are also normally fixed (only code 0000 is acceptable), but you can order any code you want by requesting a factory-mask modification.

When a valid high-order address enters the PSG, the register address (four low-order bits) is latched in the register-address/decoder block (Fig. 2). And a latched address remains valid until a new address enters the device. This means that a CPU can make multiple reads and writes of the same register contents without redundant addressing.

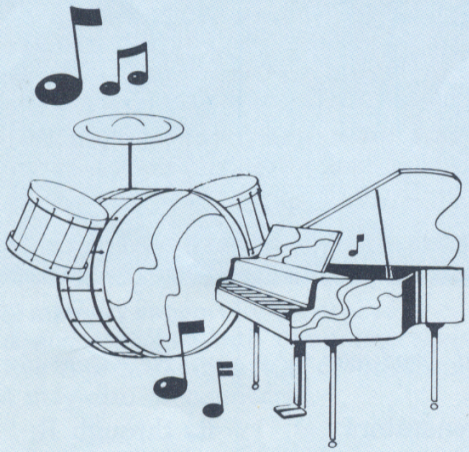
Before either the register-address/decoder or the

Music and sound effects—a combo on a chip

What your mind recognizes as music is essentially a set of mathematical relationships to a digital system like General Instrument's PSG. For example, shifting up or down in octaves can be represented by multiplying or dividing by a power of two, a simple shift operation for most microprocessors. Because the PSG operates digitally, musical notes are produced by simple register loads. Register load values create the first octave note which is shifted to the correct octave at playtime.

As good a music player as the PSG is, equally important is its sound effects capability. In fact, the chip is powerful enough to produce many sounds with just the tone generators. A tone generator sequence for a European siren effect, which is two distinct frequencies, sequentially produced, is illustrated.

Other commonly used sounds require only the noise and envelope generators. And if another channel needs the envelope generator, the system processor can control the channel envelope. An example of a sound produced with the noise and envelope generators is an explosion—it's pure noise with a decaying envelope. You can also produce a gunshot with this sequence by modifying the length of the envelope.



Siren sequence

Register #	Octal Load Value	Explanation
Any not specified	000	—
R0	376	Set channel A tone period to 2.27 ms (440 Hz).
R1	000	
R7	076	Enable tone only on channel A only.
R10	017	Select maximum amplitude on channel A.
(Wait approximately 350 ms before continuing).		
R0	126	Set channel A tone period to 5.346 ms (187).
R1	001	
(Wait approximately 350 ms before continuing).		
R10	000	Turn off channel A to end sound effect.

Explosion sequence

Register #	Octal Load Value	Explanation
Any not specified	000	—
R6	000	Set noise period to max. value.
R7	007	Enable noise only, on channels A, B, C.
R10	020	Select full amplitude range under direct control of envelope generator.
R11	020	
R12	020	
R14	070	Set envelope period 2.05 seconds.
R15	000	Select envelope "decay", one cycle only.

bidirectional buffer blocks recognize the function commanded from the bus, they must be conditioned by the bus-control decode block. Then the PSG enters one of four states: Inactive, Latch Address, Write Data or Read Data.

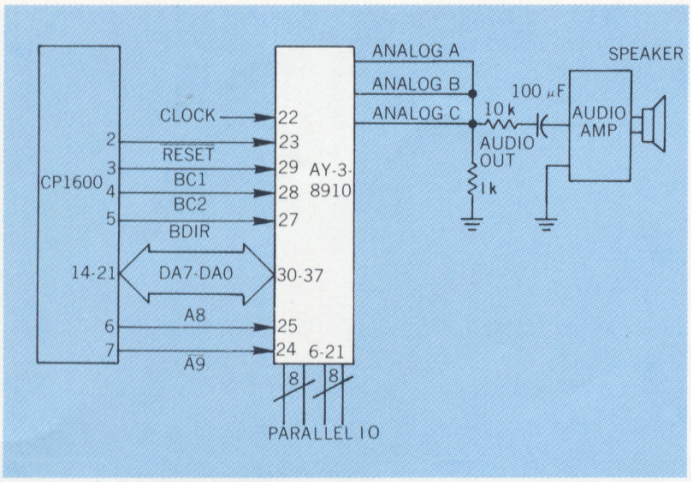
That's just the input side of the PSG. The output, which generates the programmed sounds, has its own series of functional blocks.

Sounding it out

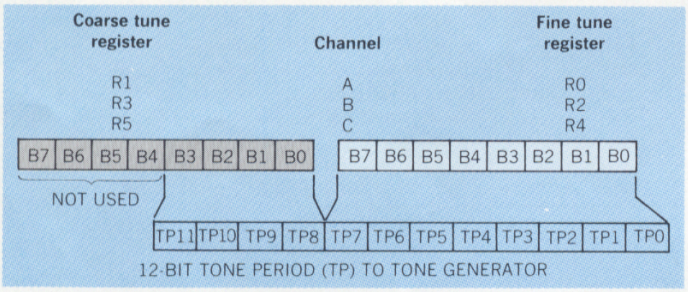
The basic blocks producing sound in the PSG are shown in Fig. 2 as:

- Tone generators to develop the basic square-wave tone frequencies for each of the three analog-output channels.
- A noise generator to produce a frequency-modulated pseudorandom-pulse-width square-wave output.
- Mixers that combine the tone-generator outputs with the noise-generator output. There's one mixer for each of the three analog-output channels.
- An envelope generator to produce a pattern that amplitude-modulates the output of each mixer.
- An amplitude control to provide internal d/a converters with either a fixed or variable-amplitude pattern. Fixed amplitude is under CPU control; variable amplitude uses the output of the envelope generator.
- Three d/a converters, each producing up to a 16-level output signal as determined by the amplitude control.

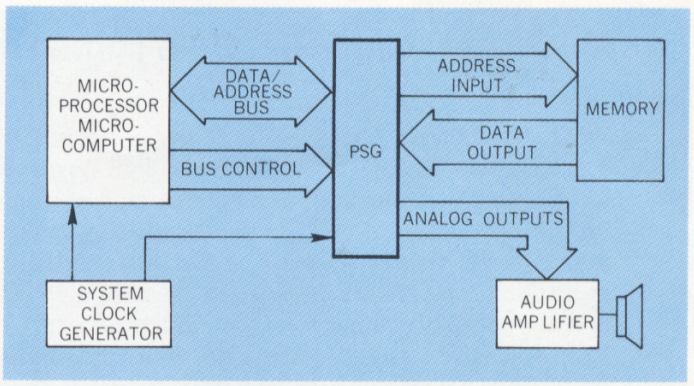
Actual sound signals for driving a speaker appear at three analog-channel outputs (channels A, B and



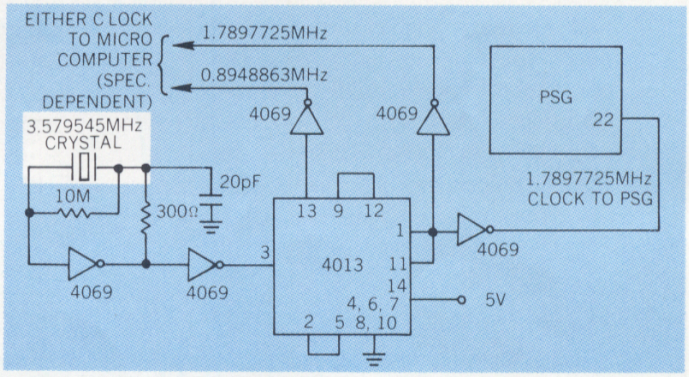
4. **A typical μP-PSG interface** requires a microprocessor, a TTL-compatible clock and just one 5-V supply. In this system, the analog-output channels are paralleled, but each channel can be driven separately.



5. **Two registers, one for coarse tuning and one for fine tuning,** are responsible for generating the PSG's 12-bit tone period. The tone period is sent to the tone-generator circuits to produce square-wave frequencies.



6. **The key elements of a PSG interface** are indicated by the white blocks in this diagram. A system clock, an audio amplifier and a microprocessor are mandatory. However, the memory block, which can be a ROM or RAM, is optional —it's only needed when a system requires additional data for processor support.



7. **Generate the system clock easily** with this simple circuit, which uses a standard color-burst crystal.

C in Fig. 2). A typical system, showing the PSG interfaced to a microprocessor, with its paralleled output channels driving a speaker is shown in Fig. 4. Each output channel provides four bits of logarithmic d/a conversion, enhancing the dynamic range of the sound. And since the analog channels can be independently programmed and driven through separate speakers, you'll be able to generate realistic sound effects.

Although the PSG's I/O ports have nothing to do with sound production, they are important to the μP-PSG communications interface. Two 8-bit ports are provided on the 40-pin AY-3-8910. The smaller AY-3-8912 (28-pins) has only one 8-bit port. All I/O port inputs are TTL-compatible, and contain internal pull-ups on each pin. The significant feature is that data going to or from a CPU can be written or read to the ports without affecting any other functions or operations of the PSG.

Now you have an over-all picture of what's inside a PSG. How it produces varied and complex sounds is another matter.

Registers call the tune

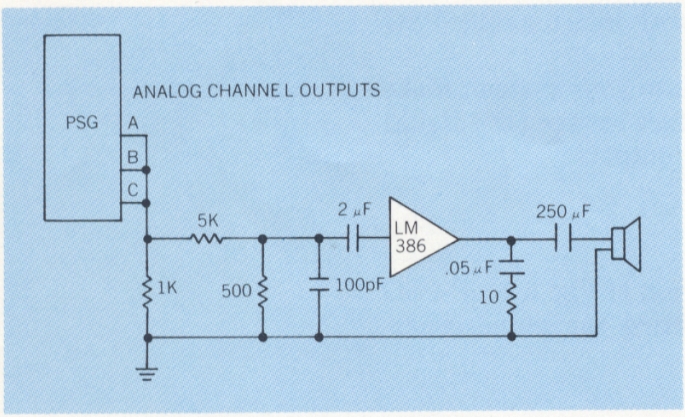
Since all PSG sound production is dictated by a host processor through commands to the 16 registers, the registers themselves are assigned to control the five actual sound producing blocks:

Sound producer	*Registers*
Tone generators	R_0 through R_5
Noise generator	R_6
Mixer control	R_7
Amplitude control	R_{10} through R_{12}
Envelope generator	R_{13} through R_{15}

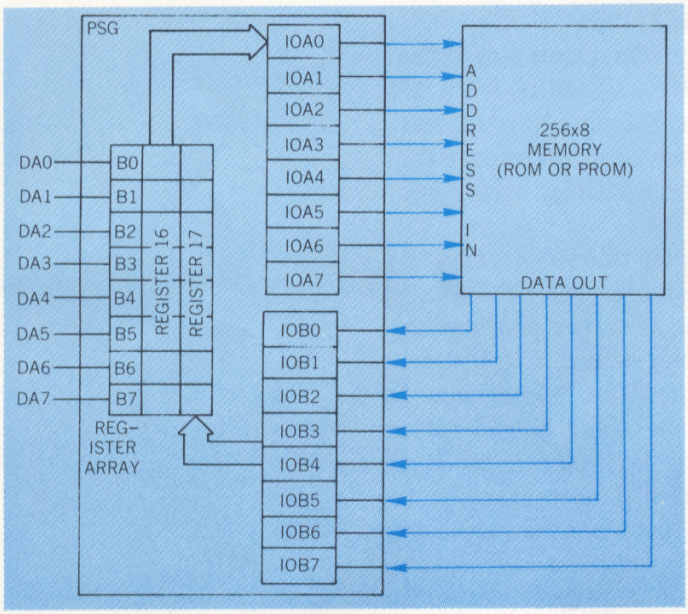
Registers R_{16} and R_{17} are responsible for controlling the two I/O ports (on the 8910 only).

By examining the tone generators' operation, you'll get an idea of how to program the other sound blocks. Each square wave produced by the three tone generators comes from dividing the input clock by 16, then counting that result down by the programmed, 12-bit tone-period value. The 12-bit value is determined by combining the contents of two registers—a coarse tune and a fine-tune register—as shown in Fig. 5.

The 12-bit result in the combined register represents a period value—the higher the value in the register, the lower the tone frequency (T = 1/f). Because of the PSG's internal count-down technique, the lowest period value is 000000000001 (divide by 1), the highest



8. **To connect an audio-interface to the sound generator,** put an LM-386 amplifier between speaker and PSG. Here the PSG outputs are summed together.



9. **External memory support** for the processor controlling the PSG is accomplished with the connections shown. Although this interface is for a ROM or PROM only, a RAM or EAROM may also be connected.

is 000000000000 (divide by 4096_{10}).

Two equations describe the relationship between the desired output tone frequency and the input clock frequency and tone period value:

$$f_t = \frac{f_{clock}}{16\ TP_{10}} \qquad (1)$$

$$TP_{10} = 256\ CT_{10} + FT_{10} \qquad (2)$$

where f_t is the desired tone frequency,

f_{clock} is the input clock frequency,

TP_{10} is the decimal equivalent of the tone period bits TP_{11} through TP_0,

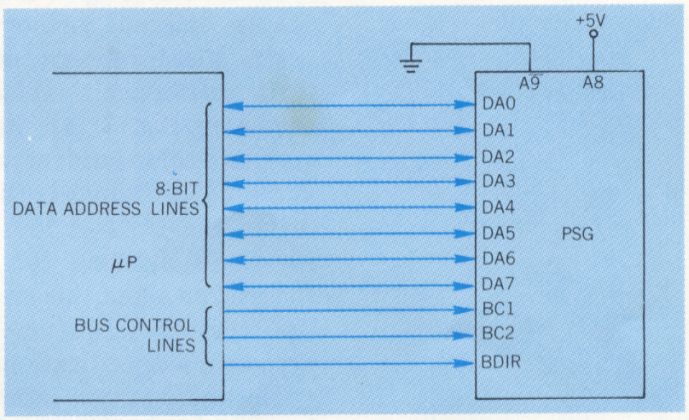
CT_{10} is the decimal equivalent of the coarse-tune-register bits B_0 through B_3 (TP_{11} through TP_8), and

FT_{10} is the decimal equivalent of the ~~coarse~~-tune-register bits B_0 through B_7 (TP_0 through TP_7).

Bus control	BDIR	BC2	BC1	Explanation of bus data (DA7--DA0)
	Bus codes			
Latch address	1	1	1	00000111: Latch R7 to program I/O ports
Write to PSG	1	1	0	01000000: Set B7, B6 to 0,1 respectively
Latch address	1	1	1	00001110: Latch R16 to address memory
Write to PSG	1	1	0	00000001: Address data to memory
Latch address	1	1	1	00001111: Latch R17 to read memory
Read from PSG	0	1	1	XXXXXXXX: Memory data contained in R17

Note: BC2 in the above Bus Codes may be permanently tied to +5V thus requiring only two bus control lines for all control operations.

10. **To address and read an external memory,** a bus-control sequence like this operates into the PSG's two 8-bit I/O ports. Note that bus code BC2 can be permanently tied to 5 V. Therefore, just two bus control lines are needed for all control operations.



11. **An 8-bit bus passes all data and address** information between PSG and processor in the μP-PSG interface. And BC1, BC2 and BDIR are the only control signals needed to direct the operations.

Equations 1 and 2 tell you that f_t has a range whose low side is $f_{clock}/65{,}536$ ($TP_{10}=4096_{10}$) and whose high side is $f_{clock}/16$ ($TP_{10} = 1$). With a 2-MHz input clock, the range of tone frequencies that you can get would be 30.5 Hz to 125 kHz.

Say you want to calculate values for the contents of the tone period's coarse and fine-tune registers. Assume you know the input clock frequency and the tone period you want to generate. First, rearrange Eqs. 1 and 2.

$$TP_{10} = \frac{f_{clock}}{16 f_t} \qquad (3)$$

$$CT_{10} + FT_{10}/256 = TP_{10}/256 \qquad (4)$$

If f_{clock} is 2 MHz and you want to generate an f_t of 100 Hz,

$$TP_{10} = \frac{2 \times 10^6}{16\ (1 \times 10^2)} = 1250$$

Substitute the value for TP_{10} into Eq. 4:

$$CT_{10} + FT_{10}/256 = 1250/256$$
$$= 4 + 226/256$$

Therefore, $CT_{10} = 4_{10} = 0100$ (B_3 through B_0)
and $FT_{10} = 226_{10} = 11100010$ (B_7 through B_0).

This calculation for tone-period register programming is similar to that required for the noise generator and envelope generator. For complete details of these blocks, plus an in-depth explanation of the amplitude control and mixer registers, d/a converter and I/O

port operation, consult General Instrument's PSG Data Manual.

Before designing the PSG into your system, make sure you understand the interface between the digital inputs and the analog sound outputs.

From input to output

As shown in the block diagram of Fig. 6, a μP-PSG interface involves interconnecting the sound generator to four subsystems:

- A clock generator.
- An audio-output interface.
- An external memory (optional).
- A microprocessor/microcomputer.

An economical way to provide a system clock is shown in Fig. 7. All you need are a 3.579545-MHz standard color-burst crystal, a CD4069 CMOS inverter and a CD4013 dual-D flip-flop. The clock signal that drives the PSG—1.7897725 MHz—results from the flip-flop's dividing the crystal frequency in half. Before you adopt this circuit however, make sure that the crystal frequency is compatible with your processor's specifications.

The audio-output interface also takes few parts and is simple to build. Fig. 8 illustrates the PSG analog channel outputs added together to drive a commercial-version LM386 IC audio amplifier, which in turn drives a speaker. The summing operation allows you to generate complex waveforms for amplification through a single speaker. On the other hand, each channel can be individually amplified for more exotic sound effects. In the PSG, output channels are separately controlled by amplitude registers R_{10}, R_{11} and R_{12} and enable register R_7 (see Fig. 2)

If you find you have to provide additional data information for processor support, you can connect an external memory to the PSG (see Fig. 9). Two on-chip registers communicate with the memory—I/O port A (8-bit) addresses it and I/O port B (also 8-bit) reads data from it.

Fig. 10 shows an example of the bus-control sequence needed to address and read an external memory. The memory is connected to the I/O ports—port A addresses and port B reads.

Depending on your design, a RAM or EAROM can replace the ROM or PROM in Fig. 9. In that case, Port B becomes the I/O and the sequence in Fig. 10 must be altered. Port B is then able to write data as an output and read data as an input. In another application, these two I/O ports could be used as switch inputs or as display outputs.

One more interface remains—the microprocessor interface. Signal lines DA_7 through DA_0 in Fig. 11 are I/O bus bits 7 through 0. All data and address information passes between the PSG and processor across this bus. Lines BC_1, BC_2 and BDIR are generated by the processor to direct all bus operations, which are identified as Latch Address, Write To PSG, Read From PSG and Inactive.■■

Commodore SID 6581 DataSheet

http://www.waitingforfriday.com/?p=661

Commodore SID 6581 Datasheet - WFFwiki

Introduction

This article is a reproduction of the original Commodore 6581 Sound Interface Device (SID) datasheet. I made this by taking a photocopy of an original document and using OCR to capture the content, then the document was hand-edited, formatted for mediawiki and reassembled here with (cleaned-up and straightened) diagrams and tables.

The reason for this was that most sources on the web are low quality PDFs and, since the documents are graphical copies of the original, they cannot be searched or indexed. The SID chip is a complex device, so I hope anyone developing projects around this device will find this mediawiki format datasheet useful.

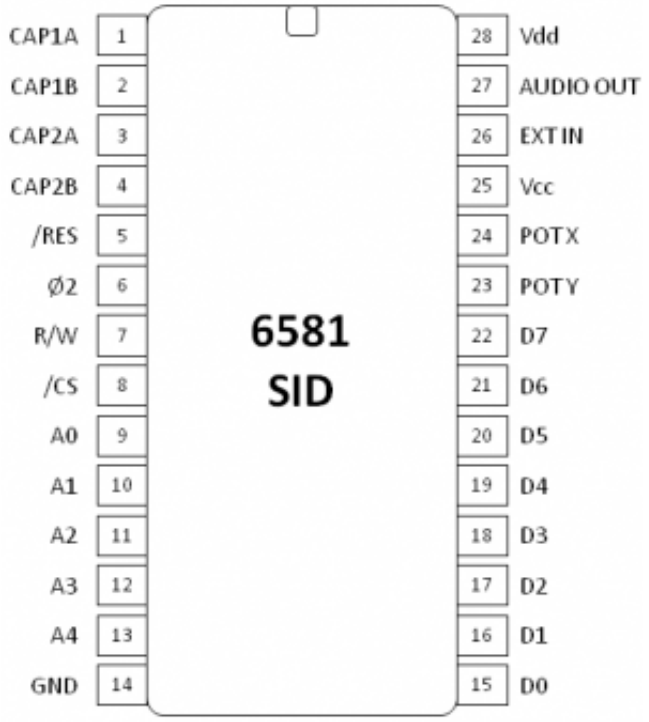
Since it was converted mainly by hand (OCR is not terribly accurate!) I would appreciate it if you could notify me of any errors or omissions you find so I can make this as accurate as possible. If you would like to make a copy of this document please note the Creative Commons licence referenced at the bottom of the page.

Concept

The 6581 Sound Interface Device (SID) is a single-chip, 3-voice electronic music synthesizer/sound effects generator compatible with the 65XX and similar microprocessor families. SID provides wide-range, high-resolution control of pitch (frequency), tone color (harmonic content) and dynamics (volume). Specialized control circuitry minimizes software overhead, facilitating use in arcade/home video games and low-cost musical instruments.

- Cutoff range: 30 Hz-12 kHz
- 12 dB/octave Rolloff
- Low pass, Band pass, High pass, Notch outputs
- Variable Resonance

6581 Pin Configuration

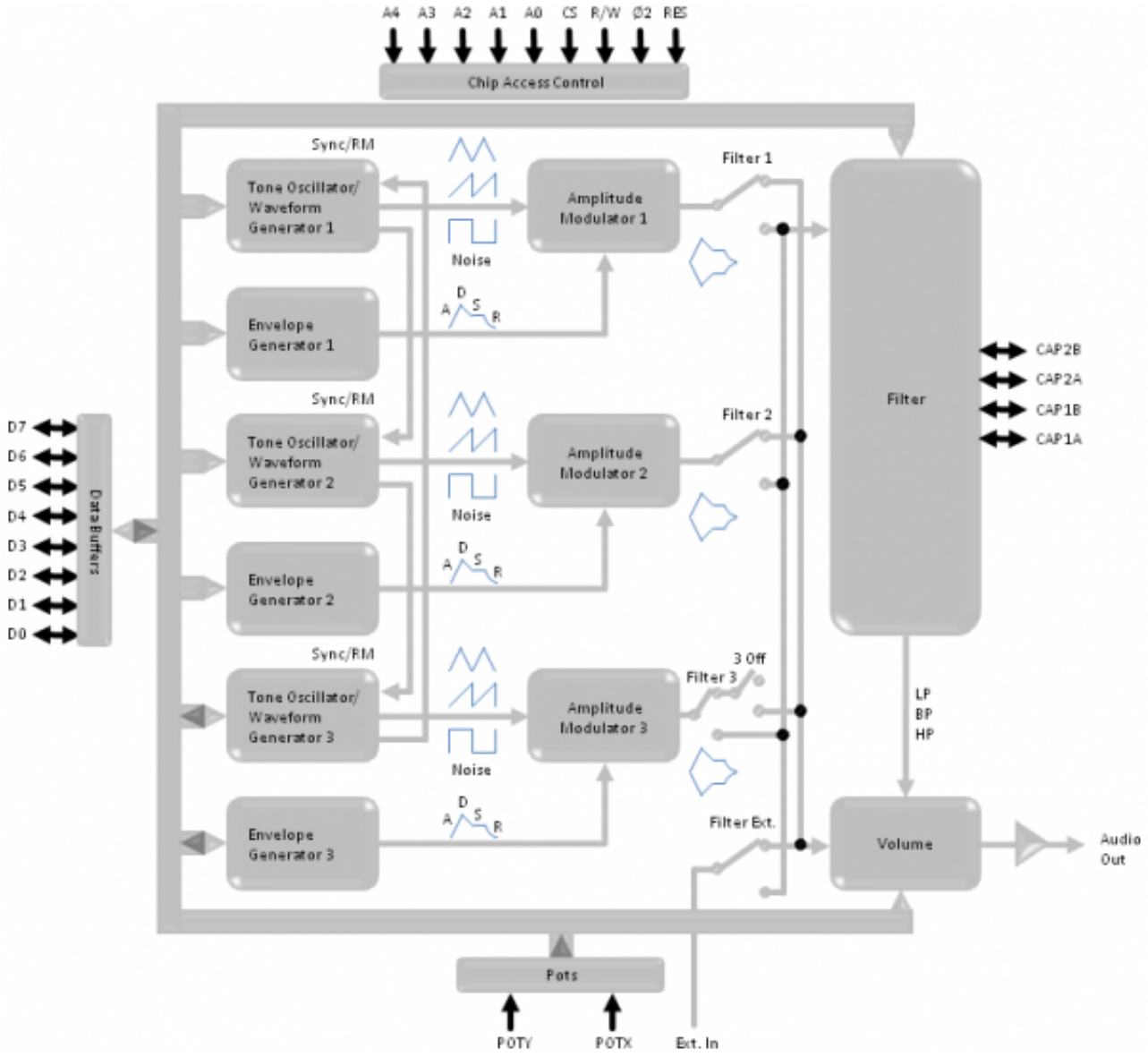


Description

The 6581 consists of three synthesizer “voices” which can be used independently or in conjunction with each other (or external audio sources) to create complex sounds. Each voice consists of a Tone Oscillator/Waveform Generator, an Envelope Generator and an Amplitude Modulator. The Tone Oscillator controls the pitch of the voice over a wide range. The Oscillator produces four waveforms at the selected frequency, with the unique harmonic content of each waveform providing simple control of tone color. The volume dynamics of the oscillator are controlled by the Amplitude Modulator under the direction of the Envelope Generator. When triggered, the Envelope Generator creates an amplitude envelope with programmable rates of increasing and decreasing volume. In addition to the three voices, a programmable Filter is provided for generating complex, dynamic tone colors via subtractive synthesis.

SID allows the microprocessor to read the changing output of the third Oscillator and third Envelope Generator. These outputs can be used as a source of modulation information for creating vibrato, frequency/filter sweeps and similar effects. The third oscillator can also act as a random number generator for games. Two A/D converters are provided for interfacing SID with potentiometers. These can be used for “paddles” in a game environment or as front panel controls in a music synthesizer. SID can process external audio signals, allowing multiple SID chips to be daisy-chained or mixed in complex polyphonic systems.

6581 SID Block Diagram



SID Control Registers

There are 29 eight-bit registers in SID which control the generation of sound. These registers are either WRITE-only or READ-only and are listed below in Table 1.

	Address					Reg #	Data									
	A4	A3	A2	A1	A0	(Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Reg Name	Reg Type
															VOICE 1	
0	0	0	0	0	0	00	F7	F6	F5	F4	F3	F2	F1	F0	Freq Lo	Write-only
1	0	0	0	0	1	01	F15	F14	F13	F12	F11	F10	F9	F8	Freq Hi	Write-only
2	0	0	0	1	0	02	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	PW LO	Write-only
3	0	0	0	1	1	03	—	—	—	—	PW11	PW10	PW9	PW8	PW HI	Write-only
4	0	0	1	0	0	04	NOISE	⊓⊔	◿	∧	TEST	RING MOD	SYNC	GATE	Control Reg	Write-only
5	0	0	1	0	1	05	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0	Attack/Decay	Write-only
6	0	0	1	1	0	06	STN3	STN2	STN1	STN0	RIS3	RIS2	RIS1	RIS0	Sustain/Release	Write-only
															VOICE 2	
7	0	0	1	1	1	07	F7	F6	F5	F4	F3	F2	F1	F0	Freq LO	Write-only
8	0	1	0	0	0	08	F15	F14	F13	F12	F11	F10	F9	F8	Freq Hi	Write-only
9	0	1	0	0	1	09	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	PW LO	Write-only
10	0	1	0	1	0	0A	—	—	—	—	PW11	PW10	PW9	PW8	PW HI	Write-only
11	0	1	0	1	1	0B	NOISE	⊓⊔	◿	∧	TEST	RING MOD	SYNC	GATE	Control Reg	Write-only
12	0	1	1	0	0	0C	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0	Attack/Decay	Write-only
13	0	1	1	0	1	0D	STN3	STN2	STN1	STN0	RIS3	RIS2	RIS1	RIS0	Sustain/Release	Write-only
															VOICE 3	
14	0	1	1	1	0	0E	F7	F6	F5	F4	F3	F2	F1	F0	Freq Lo	Write-only
15	0	1	1	1	1	0F	F15	F14	F13	F12	F11	F10	F9	F8	Freq Hi	Write-only
16	1	0	0	0	0	10	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	PW LO	Write-only
17	1	0	0	0	1	11	—	—	—	—	PW11	PW10	PW9	PW8	PW HI	Write-only
18	1	0	0	1	0	12	NOISE	⊓⊔	◿	∧	TEST	RING MOD	SYNC	GATE	Control Reg	Write-only
19	1	0	0	1	1	13	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0	Attack/Decay	Write-only
20	1	0	1	0	0	14	STN3	STN2	STN1	STN0	RIS3	RIS2	RIS1	RIS0	Sustain/Release	Write-only
															Filter	
21	1	0	1	0	1	15	—	—	—	—	—	FC2	FC1	FC0	FC LO	Write-only
22	1	0	1	1	0	16	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC HI	Write-only
23	1	0	1	1	1	17	RES3	RES2	RES1	RES0	Filt EX	Filt 3	Filt 2	Filt 1	RES/Filt	Write-only
24	1	1	0	0	0	18	3 OFF	HP	BP	LP	VOL3	VOL2	VOL1	VOL0	Mode/Vol	Write-only
															Misc	
25	1	1	0	0	1	19	PX7	PX6	PX5	PX4	PX3	PX2	PX1	PX0	POTX	Read-only
26	1	1	0	1	0	1A	PY7	PY6	PY5	PY4	PY3	PY2	PY1	PY0	POTY	Read-only
27	1	1	0	1	1	1B	07	06	05	04	03	02	01	00	OSC3/Random	Read-only
28	1	1	1	0	0	1C	E7	E6	E5	E4	E3	E2	E1	E0	ENV3	Read-only

Table 1

SID Register Description

Voice 1

Freq Lo/Freq Hi (Registers 00-01)

Together these registers form a 16-bit number which linearly controls the Frequency of Oscillator 1. The frequency is determined by the following equation:

Fout = (Fn * Fclk/16777216) Hz

Where Fn is the 16-bit number in the Frequency registers and Fclk is the system clock applied to the Ø2 input (pin 6). For a standard 1.0 Mhz clock, the frequency is given by:

Fout = (Fn * 0.0596) Hz

A complete table of values for generating 8 octaves of the equally-tempered musical scale with concert A

(440 Hz) tuning is provided in Appendix A. It should be noted that the frequency resolution of SID is sufficient for any tuning scale and allows sweeping from note to note (portamento) with no discernible frequency steps.

PW Lo/PW Hi (Registers 02-03)

Together these registers form a 12-bit number (bits 4-7 of PW Hi are not used) which linearly controls the Pulse Width (duty cycle) of the Pulse waveform on Oscillator 1. The pulse width is determined by the following equation:

PWout = (PWn/40.95) %

Where PWn is the 12-bit number in the Pulse Width registers.

The pulse width resolution allows the width to be smoothly swept with no discernible stepping. Note that the Pulse waveform on Oscillator 1 must be selected in order for the Pulse Width registers to have any audible effect. A value of 0 or 4095 ($FFF) in the Pulse Width registers will produce a constant DC output, while a value of 2048 ($800) will produce a square wave.

Control Register (Register 04)

This register contains eight control bits which select various options on Oscillator 1.

Gate (Bit 0)

The GATE bit controls the Envelope Generator for Voice 1. When this bit is set to a one, the Envelope Generator is Gated (triggered) and the ATTACK/DECAY/SUSTAIN cycle is initiated. When the bit is reset to a zero, the RELEASE cycle begins. The Envelope Generator controls the amplitude of Oscillator 1 appearing at the audio output, therefore, the GATE bit must be set (along with suitable envelope parameters) for the selected output of Oscillator 1 to be audible. A detailed discussion of the Envelope Generator can be found in Appendix B.

Sync (Bit 1)

The SYNC bit, when set to a one, Synchronizes the fundamental frequency of Oscillator 1 with the fundamental frequency of Oscillator 3, producing “Hard Sync” effects. Varying the frequency of Oscillator 1 with respect to Oscillator 3 produces a wide range of complex harmonic structures from Voice 1 at the frequency of Oscillator 3. In order for sync to occur Oscillator 3 must be set to some frequency other than zero but preferably lower than the frequency of Oscillator 1. No other parameters of Voice 3 have any effect on sync.

Ring Mod (Bit 2)

The RING MOD bit, when set to a one, replaces the Triangle waveform output of Oscillator 1 with a “Ring

Modulated" combination of Oscillators 1 and 3. Varying the frequency of Oscillator 1 with respect to Oscillator 3 produces a wide range of non-harmonic overtone structures for creating bell or gong sounds and for special effects. In order for ring modulation to be audible, the Triangle waveform of Oscillator 1 must be selected and Oscillator 3 must be set to some frequency other than zero. No other parameters of Voice 3 have any effect on ring modulation.

Test (Bit 3)

The TEST bit, when set to a one, resets and locks Oscillator 1 at zero until the TEST bit is cleared. The Noise waveform output of Oscillator 1 is also reset and the Pulse waveform output is held at a DC level. Normally this bit is used for testing purposes, however, it can be used to synchronize Oscillator 1 to external events, allowing the generation of highly complex waveforms under real-time software control.

Triangle Wave (Bit 4)

When set to a one, the Triangle waveform output of Oscillator 1 is selected. The Triangle waveform is low in harmonics and has a mellow, flute-like quality.

Sawtooth Wave (Bit 5)

When set to a one, the Sawtooth waveform of Oscillator 1 is selected. The sawtooth waveform is rich in even and odd harmonics and has a bright, brassy quality.

Square Wave (Bit 6)

When set to a one, the Pulse waveform output of Oscillator 1 is selected. The harmonic content of this waveform can be adjusted by the Pulse Width registers, producing tone Qualities ranging from a bright, hollow square wave to a nasal, reedy pulse. Sweeping the pulse width in real-time produces a dynamic "phasing" effect which adds a sense of motion to the sound. Rapidly jumping between different pulse widths can produce interesting harmonic sequences.

Noise (Bit 7)

When set to a one, the Noise output waveform of Oscillator 1 is selected. This output is a random signal which changes at the frequency of Oscillator 1. The sound quality can be varied from a low rumbling to hissing white noise via the Oscillator 1 Frequency registers. Noise is useful in creating explosions, gunshots, jet engines, wind, surf and other un-pitched sounds, as well as snare drums and cymbals. Sweeping the Oscillator frequency with Noise selected produces a dramatic rushing effect. One of the output waveforms must be selected for Oscillator 1 to be audible, however it is NOT necessary to deselect waveforms to silence the output of Voice 1. The amplitude of Voice 1 at the final output is a function of the Envelope Generator only.

NOTE: The oscillator output waveforms are NOT additive. If more than one output waveform is selected

simultaneously, the result will be a logical ANDing of the waveforms. Although this technique can be used to generate additional waveforms beyond the four listed above, it must be used with care. If any other waveform is selected while Noise is on, the Noise output can “lock up”. If this occurs, the Noise output will remain silent until reset by the TEST bit or by bringing /RES (pin 5) low.

Attack/Decay (Register 05)

Bits 4-7 of this register (ATK0-ATK3) select 1 of 16 ATTACK rates for the Voice 1 Envelope Generator. The ATTACK rate determines how rapidly the output of Voice 1 rises from zero to peak amplitude when the Envelope Generator is Gated. The 16 ATTACK rates are listed below in Table 2.

Bits 0-3 (DCY0-DCY3) select 1 of 16 DECAY rates for the Envelope Generator. The DECAY cycle follows the ATTACK cycle and the DECAY rate determines how rapidly the output falls from the peak amplitude to the selected SUSTAIN level. The 16 DECAY rates are listed in Table 2.

		Attack Rate	**Release Rate**
DEC	**HEX**	**(Time/Cycle)**	**(Time/Cycle)**
0	(0)	2 mS	6 mS
1	(1)	8 mS	24 mS
2	(2)	16 mS	48 mS
3	(3)	24 mS	72 mS
4	(4)	38 mS	114 mS
5	(5)	56 mS	168 mS
6	(6)	68 mS	204 mS
7	(7)	80 mS	240 mS
8	(8)	100 mS	300 mS
9	(9)	250 mS	750 mS
10	(A)	500 mS	1.5 S
11	(B)	800 mS	2.4 S
12	(C)	1 S	3 S
13	(D)	3 S	9 S

14	(E)	5 S	15 S
15	(F)	8 S	24 S

Table 2

NOTE: Envelope rates are based on a 1.0 Mhz Ø2 clock. For other Ø2 frequencies, multiply the given rate by 1 Mhz / Ø2. The rates refer to the amount of time per cycle. For example, given an ATTACK value of 2, the ATTACK cycle would take 16 mS to rise from zero to peak amplitude. The DECAY/RELEASE rates refer to the amount of time these cycles would take to fall from peak amplitude to zero.

Sustain/Release (Register 06)

Bits 4-7 of this register (STN0-STN3) select 1 of 16 SUSTAIN levels for the Envelope Generator. The SUSTAIN cycle follows the DECAY cycle and the output of Voice 1 will remain at the selected SUSTAIN amplitude as long as the Gate bit remains set. The SUSTAIN levels range from zero to peak amplitude in 16 linear steps, with a SUSTAIN value of 0 selecting zero amplitude and a SUSTAIN value of 15 (#F) selecting the peak amplitude.

A SUSTAIN value of 8 would cause Voice 1 to SUSTAIN at an amplitude one-half the peak amplitude reached by the ATTACK cycle.

Bits 0-3 (RLS0-RLS3) select 1 of 16 RELEASE rates for the Envelope Generator. The RELEASE cycle follows the SUSTAIN cycle when the Gate bit is reset to zero. At this time, the output of Voice 1 will fall from the SUSTAIN amplitude to zero amplitude at the selected RELEASE rate. The 16 RELEASE rates are identical to the DECAY rates.

NOTE: The cycling of the Envelope Generator can be altered at any point via the Gate bit. The Envelope Generator can be Gated and Released without restriction. For example, if the Gate bit is reset before the envelope has finished the ATTACK cycle, the RELEASE cycle will immediately begin, starting from whatever amplitude had been reached. If the envelope is then Gated again (before the RELEASE cycle has reached zero amplitude), another ATTACK cycle will begin, starting from whatever amplitude had been reached. This technique can be used to generate complex amplitude envelopes via real-time software control.

Voice 2

Registers 07-$0D control Voice 2 and are functionally identical to registers 00-06 with these exceptions:

When selected, SYNC synchronizes Oscillator 2 with Oscillator 1.

When selected, RING MOD replaces the Triangle output of Oscillator 2 with the ring modulated combination of Oscillators 2 and 1.

Voice 3

Registers $0E-$14 control Voice 3 and are functionally identical to registers 00-06 with these exceptions:

When selected, SYNC synchronizes Oscillator 3 with Oscillator 2.

When selected, RING MOD replaces the Triangle output of Oscillator 3 with the ring modulated combination of Oscillators 3 and 2.

Typical operation of a voice consists of selecting the desired parameters: frequency, waveform effects (SYNC, RING MOD) and envelope rates, then gating the voice whenever the sound is desired. The sound can be sustained for any length of time and terminated by clearing the Gate bit. Each voice can be used separately, with independent parameters and gating, or in unison to create a single, powerful voice. When used in unison, a slight detuning of each oscillator or tuning to musical intervals creates a rich, animated sound.

Filter

FC Lo/FC Hi (Registers $15, $16)

Together these registers form an 11-bit number (bits 3-7 of FC LO are not used) which linearly controls the Cutoff (or Center) Frequency of the programmable Filter. The approximate Cutoff Frequency ranges between 30Hz and 10KHz with the recommended capacitor values of 2200pF for CAP1 and CAP2. The frequency range of the Filter can be altered to suit specific applications. Refer to the Pin Description section for more information.

RES/Filt (Register $17)

Bits 4-7 of this register (RES0-RES3) control the Resonance of the Filler, resonance of a peaking effect which emphasizes frequency components at the Cutoff Frequency of the Filter, causing a sharper sound. There are 16 Resonance settings ranging linearly from no resonance (0) to maximum resonance (15 or #F).

Bits 0-3 determine which signals will be routed through the Filter:

Filt 1 (Bit 0)

When set to a zero, Voice 1 appears directly at the audio output and the Filter has no effect on it. When set to a one, Voice 1 will be processed through the Filter and the harmonic content of Voice 1 will be altered according to the selected Filter parameters.

Filt 2 (Bit 1)

Same as bit 0 for Voice 2.

Filt 3 (Bit 2)

Same as bit 0 for voice 3.

Filtex (Bit 3)

Same as bit 0 for External audio input (pin 26).

Mode/Vol (Register $18)

Bits 4-7 of this register select various Filter mode and output options:

LP (Bit 4)

When set to a one, the low Pass output of the Filter is selected and sent to the audio output. For a given Filter input Signal, all frequency components below the Filter Cutoff Frequency are passed unaltered, while all frequency components above the Cutoff are attenuated at a rate of 12 dB/Octave. The low Pass mode produces full-bodied sounds.

BP (Bit 5)

Same as bit 4 for the Band Pass output. All frequency components above and below the Cutoff are attenuated at a rate of 6 dB/Octave. The Band Pass mode produces thin, open sounds.

HP (Bit 6)

Same as bit 4 for the High Pass output. All frequency components above the Cutoff are passed unaltered, while all frequency components below the Cutoff are attenuated at a rate of 12 dB/Octave. The High Pass mode produces tinny, buzzy sounds.

3 OFF (Bit 7)

When set to a one, the output of Voice 3 is disconnected from the direct audio path. Setting Voice 3 to bypass the Filter (FILT 3 = 0) and selling 3 OFF to a one prevents Voice 3 from reaching the audio output. This allows Voice 3 to be used for modulation purposes without any undesirable output.

NOTE: The Filter output modes ARE additive and multiple Filter modes may be selected simultaneously.

For example, both LP and HP modes can be selected to produce a Notch (or Band Reject) Filter response. In order for the Filter to have any audible effect, at least one Filter output must be selected and at least one Voice must be routed through the Filter. The Filter is, perhaps, the most important element in SID as it allows the generation of complex tone colors via subtractive synthesis. The Filter is used to eliminate specific frequency components from a harmonically-rich input signal). The best results are achieved by varying the Cutoff Frequency in real-time.

Bits 0-3 (VOL0-VOL3) select 1 of 16 overall Volume levels for the final composite audio output. The output volume levels range from no output (0) to maximum volume (15 or #F) in 16 linear steps. This control can be used as a static volume control for balancing levels in multi-chip systems or for creating dynamic volume effects, such as Tremolo. Some Volume level other than zero must be selected in order for SID to produce any sound.

Misc

POTX (Register $19)

This register allows the microprocessor to read the position of the potentiometer tied to POTX (pin 24), with values ranging from 0 at minimum resistance, to 255 (#FF) at maximum resistance. The value is always valid and is updated every 512 Ø2 clock cycles. See the Pin Description section for information on post and capacitor values.

POTY (Register $1A)

Same as POTX for the pot tied to POTY (pin 23).

OSC 3/RANDOM (Register $1B)

This register allows the microprocessor to read the upper 8 output bits of Oscillator 3. The character of the numbers generated is directly related to the waveform selected. If the Sawtooth waveform of Oscillator 3 is selected, this register will present a series of numbers incrementing from 0 to 255 ($FF) at a rate determined by the frequency of Oscillator 3. If the Triangle waveform is selected, the output will increment from 0 up to 255, then decrement down to 0. If the Pulse waveform is selected, the output will jump between 0 and 255. Selecting the Noise waveform will produce a series of random numbers, therefore, this register can be used as a random number generator for games. There are numerous timing and sequencing applications for the OSC 3 register, however, the chief function is probably that of a modulation generator. The numbers generated by this register can be added, via software, to the Oscillator or Filter Frequency registers or the Pulse Width registers in real-time. Many dynamic effects can be generated in this manner. Siren-like sounds can be created by adding the OSC 3 Sawtooth output to the frequency control of another oscillator. Synthesizer “Sample and Hold” effects can be produced by adding the OSC 3 Noise output to the Filter Frequency control registers. Vibrato can be produced by selling Oscillator 3 to a frequency around 7 Hz and adding the OSC 3 Triangle output (with proper scaling) to the Frequency control of another oscillator. An unlimited range of effects are available by altering the frequency of Oscillator 3 and scaling the OSC 3 output. Normally, when Oscillator 3 is used for modulation, the audio output of Voice 3 should be eliminated (3 OFF = 1).

ENV 3 (Register $1C)

Same as OSC 3, but this register allows the microprocessor to read the output of the Voice 3 Envelope Generator. This output can be added to the Filler Frequency to produce harmonic envelopes, WAH WAH,

and similar effects. “Phaser” sounds can be created by adding this output to the frequency control registers of an oscillator. The Voice 3 Envelope Generator must be gated in order to produce any output from this register. The OSC 3 register, however, always reflects the changing output of the oscillator and is not affected in any way by the Envelope Generator.

SID Pin Description

CAP1A, CAP1B (Pins 1,2)/CAP2A, CAP2B Pins 3,4)

These pins are used to connect the two integrating capacitors required by the programmable Filter. C1 connects between pins 1 and 2, C2 between pins 3 and 4. Both capacitors should be the same value. Normal operation of the Filter over the audio range (approximately - 30 Hz-12 KHz) is accomplished with a value of 2200 pF for C1 and C2. Polystyrene capacitors are preferred. In complex polyphonic systems, where many SID chips must track each other, matched capacitors are recommended. The frequency range of the Filter can be tailored to specific applications by the choice of capacitor values. For example, a low-cost game may not require full high-frequency response, In this case, larger values for C1 and C2 could be chosen to provide more control over the bass frequencies of the Filter. The approximate maximum Cutoff Frequency of the Filter is given by:

FCmax = 2.6E-5/C

Where C is the capacitor value. The range of the Filter extends approximately 9 octaves below the maximum Cutoff Frequency.

/RES (Pin 5) -This TTL-level input is the reset control for SID. When brought low for at least ten Ø2 cycles, all internal registers are reset to zero and the audio output is silenced. This pin is normally connected to the reset line of the microprocessor or a power-on-clear circuit.

Ø2 (Pin 6) -This TTL-level input is the master clock for SID. All oscillator frequencies and envelope rates are referenced to this clock. Ø2 also controls data transfers between SID and the microprocessor. Data can only be transferred when Ø2 is high. Essentially, Ø2 acts as a high-active chip select as far as data transfers are concerned. This pin is normally connected to the system clock, with a nominal operating frequency of 1.0 MHz.

R/W (Pin 7) -This TTL-level input controls the direction of data transfers between SID and the microprocessor. If the chip select conditions have been met, a high on this line allows the microprocessor to Read data from the selected SID register and a low allows the microprocessor to Write data into the selected SID register. This pin is normally connected to the system Read/Write line.

/CS (Pin 8) -This TTL-level input is a low active Chip select which controls data transfers between SID and the microprocessor. /CS must be low for any transfer. A Read from the selected SID register can only occur if /CS is low, Ø2 is high and R/W is high. A Write to the selected SID register can only occur if /CS is low,

Ø2 is high and R/W is low. This pin is normally connected to address decoding circuitry, allowing SID to reside in the memory map of a system.

A0-A4 (Pins 9-13) -These TTL-level inputs are used to select one of the 29 SID registers. Although enough addresses are provided to select 1 of 32 registers, the remaining three register locations are not used. A Write to any of these three locations is ignored and a Read returns invalid data. These pins are normally connected to the corresponding address lines of the microprocessor so that SID may be addressed in the same manner as memory.

GND (Pin 14) -For best results, the ground line between SID and the power supply should be separate from ground tines to other digital circuitry. This will minimize digital noise at the audio output.

D0-D7 (Pins 15-22) -These bidirectional lines are used to transfer data between SID and the microprocessor. They are TTL compatible in the output mode and capable of driving 2 TTL loads in the output mode. The data buffers are usually in the high-impedance off state. During a Write operation, the data buffers remain in the off (input) state and the microprocessor supplies data to SID over these lines. During a Read operation, the data buffers turn on and SID supplies data to the microprocessor over these lines. The pins are normally connected to the corresponding data lines of the microprocessor.

POTX, POTY (Pins 24, 23) -These pins are inputs to the A/D converters used to digitize the position of potentiometers. The conversion process is based on the time constant of a capacitor tied from the POT pin to ground, charged by a potentiometer tied from the POT pin to +5 volts. The component values are determined by

RC = 4.7E-4

Where R is the maximum resistance of the pot and C is the capacitor.

The larger the capacitor, the smaller the POT value jitter. The recommended values for R and C are 470 KOhms and 1000 pF.

Note that a separate pot and cap are required for each POT pin.

Vcc (Pin 25) - As with the GND line, a separate +5 VDC line should be run between SID Vcc and the power supply in order to minimize noise. A bypass capacitor should be located close to the pin.

Ext In (Pin 26) -This analog input allows external audio signals to be mixed with the audio output of SID or processed through the Filter. Typical sources include voice, guitar and organ. The input impedance of this pin is in the order of 100 KOhms. Any signal applied directly to the pin should ride at DC level of 6 volts and should not exceed 3 volts p-p. In order to prevent any interference caused by DC level differences, external signals should be AC-coupled to EXT IN by an electrolytic capacitor in the 1-10uF range. As the direct audio path (FILTEX = 0) has unity gain, EXT IN can be used to mix outputs of many SID chips by daisy-chaining. The number of chips that can be chained in this manner is determined by the amount of noise

and distortion allowable at the final output. Note that the output Volume control will affect not only the three SID voices, but also any external inputs.

Audio Out (Pin 27) -This open-source buffer is the final audio output of SID, comprised of the three SID voices, the Filter and any external input. The output level is set by the output Volume control and reaches a maximum of approximately 3 volts p-p at a 6 volt DC level. A source resistor from AUDIO OUT to ground is required for proper operation. The recommended resistance is 1 KOhm for a standard output impedance. As the output of SID rides at a 6 volt DC level, it should be AC-coupled to any audio amplifier with an electrolytic capacitor in the 1-10uF range.

Vdd (Pin 28) - As with Vcc, a separate + 12 VDC fine should be run to SID Vdd and a bypass capacitor should be used.

See Appendix C for typical SID application.

6581 SID Characteristics

Absolute Maximum Ratings

- Supply Voltage, Vdd -0.3 VDC to +17 VDC
- Supply Voltage, Vcc -0.3 VDC to +7 VDC
- Input Voltage (analog). Vina -0.3 VDC to +17 VDC
- Input Voltage (digital), Vind -0.3 VDC to +7 VDC
- Operating Temperature, Ta 0° C to +70° C
- Storage Temperature, Tstg -55° C to +150° C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

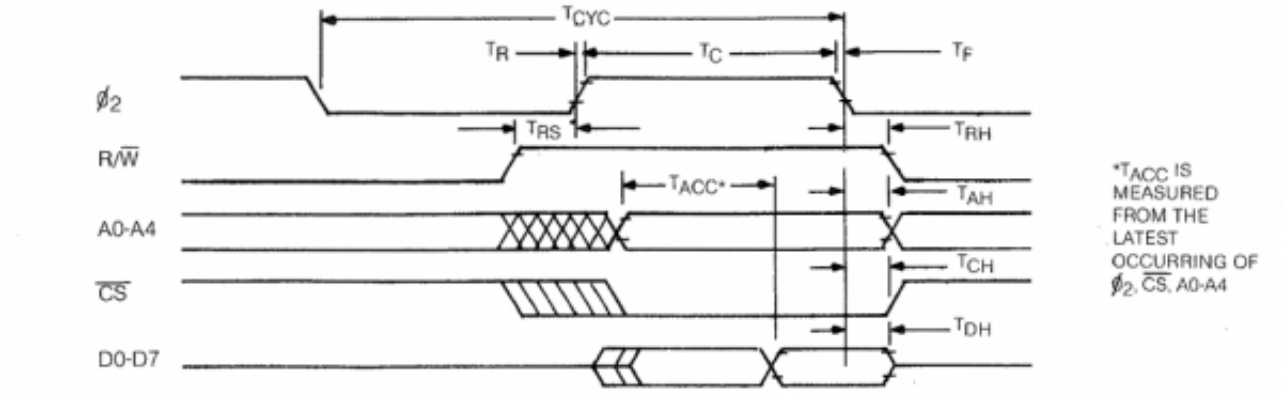
Comment

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Vdd=12±5% VDC / Vcc=5±5% VDC. Ta=0 to 70°C)						
Characteristic		**Symbol**	**Min**	**Typ**	**Max**	**Units**
Input High Voltage	($\overline{RES}$, Ø2, R/$\overline{W}$, $\overline{CS}$,	V_{ih}	2	—	Vcc	VDC
Input Low Voltage	A0-A4, D0-D7)	V_{il}	−0.3	—	0.8	VDC
Input Leakage Current	($\overline{RES}$, Ø2, R/$\overline{W}$, $\overline{CS}$, A0-A4; Vin=0-5 VDC)	I_{in}	—	—	2.5	µA
Three-State (Off) Input Leakage Current	(D0-D7; Vcc=max, Vin=0.4-2.4 VDC)	I_{tsi}	—	—	10	µA
Output High Voltage	D0-D7; Vcc=min, I load=200 µA)	V_{oh}	2.4	—	Vcc-0.7	VDC
Output Low Voltage	(D0-D7; Vcc=max, I load=3.2 mA)	V_{ol}	GND	—	0.4	VDC
Output High Current	(D0-D7; Sourcing, Voh=2.4 VDC)	I_{oh}	200	—	—	µA
Output Low Current	(D0-D7; Sinking, Vol=0.4 VDC)	I_{ol}	3.2	—	—	mA
Input Capacitance	($\overline{RES}$, Ø2, R/$\overline{W}$, $\overline{CS}$, A0-A4, D0-D7)	C_{in}	—	—	10	pF
Pot Trigger Voltage	(POTX, POTY)	V_{pot}	—	Vcc/2	—	VDC
Pot Sink Current	(POTX, POTY)	I_{pot}	500	—	—	µA
Input Impedance	(EXT IN)	R_{in}	100	150	—	KOhms
Audio Input Voltage	(EXT IN)	V_{in}	5.0 —	6.0 0.3	7.5 3	VDC VAC
Audio Output Voltage	(AUDIO OUT; 1 KOhm load, volume=max) One Voice on: All Voices on:	5.0 Vout	6.5 5.0 .25 .75	8.0 6.5 .8 3	8.0 1.2 .4	VDC VACp-p VACp-p
Power Supply Current	(Vdd)	Idd	—	25	40	mA
Power Supply Current	(Vcc)	Icc	—	70	100	mA
Power Dissipation	(Total)	Pd	—	600	1000	mW

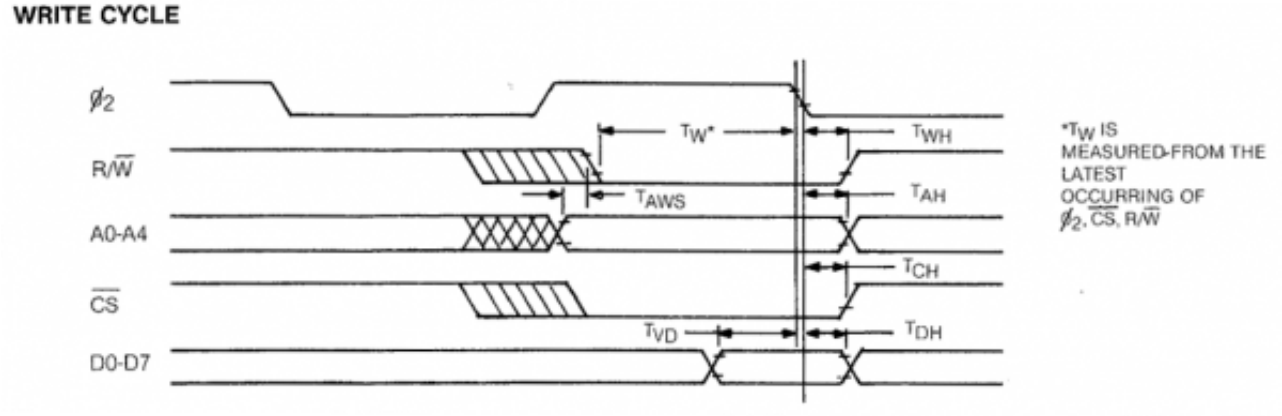
6581 (SID) Timing

READ CYCLE



Symbol	Name	Min	Typ	Max	Units
T_{CYC}	Clock Cycle Time	1	—	20	uS
T_C	Clock High Pulse Width	450	500	10,000	nS
T_R, T_F	Clock Rise/Fall Time	—	—	25	nS
T_{RS}	Read Set-up Time	0	—	—	nS
T_{RH}	Read Hold Time	0	—	—	nS
T_{ACC}	Access Time	—	—	350	nS
T_{AH}	Address Hold Time	10	—	—	nS
T_{CH}	Chip Select Hold Time	0	—	—	nS
T_{DH}	Data Hold Time	20	—	—	nS

WRITE CYCLE



Symbol	Name	Min	Typ	Max	Units
T_W	Write Pulse Width	350	—	—	nS
T_{WH}	Write Hold Time	0	—	—	nS
T_{AWS}	Address Set-up Time	0	—	—	nS
T_{AH}	Address Hold Time	10	—	—	nS
T_{CH}	Chip Select Hold Time	0	—	—	nS
T_{VD}	Valid Data	80	—	—	nS
T_{DH}	Data Hold Time	10	—	—	nS

Appendix A - Equal-Tempered Musical Scale Values

The following table lists the numerical values which must be stored in the SID Oscillator frequency control registers to produce the notes of the equal-tempered musical scale. The equal-tempered scale consists of an octave containing 12 semitones (notes): C, D, E, F, G, A, B and C#, D#, F#, G#, A#. The frequency of each semitone is exactly the 12th root of 2 times the frequency of the previous semitone. The table is based on a Ø2 = clock of 1.0 Mhz. Refer to the equation given in the Register Description for use of other master clock frequencies. The scale selected is concert pitch, in which A4 = 440 Hz. Transpositions of this scale and scales other than the equal-tempered scale are also possible.

	Musical Note	Freq (Hz)	Osc Fn (Decimal)	Osc Fn (Hex)		Musical Note	Freq (Hz)	Osc Fn (Decimal)	Osc Fn (Hex)
1	C0$	17.32	291	0123	49	C4$	277.18	4650	122A
2	D0	18.35	308	0134	50	D4	293.66	4927	133F
3	D0$	19.44	326	0146	51	D4$	311.13	5220	1464
4	E0	20.60	346	015A	52	E4	329.63	5530	159A
5	F0	21.83	366	016E	53	F4	349.23	5859	16E3
6	F0$	23.12	388	0184	54	F4$	370.00	6207	183F
7	G0	24.50	411	018B	55	G4	392.00	6577	1981

8	G0$	25.96	435	01B3	56	G4$	415.30	6968	1B38
9	A0	27.50	461	01CD	57	A4	440.00	7382	1CD6
10	A0$	29.14	489	01E9	58	A4$	466.16	7821	1E80
11	B0	30.87	518	0206	59	B4	493.88	8286	205E
12	C1	32.70	549	0225	60	C5	523.25	8779	224B
13	C1$	34.65	581	0245	61	C5$	554.37	9301	2455
14	D1	36.71	616	0268	62	D5	587.33	9854	267E
15	D1$	38.89	652	028C	63	D5$	622.25	10440	28C8
16	E1	41.20	691	02B3	64	E5	659.25	11060	2B34
17	F1	43.65	732	02DC	65	F5	698.46	11718	2DC6
18	F1$	46.25	776	0308	66	F5$	740.00	12415	307F
19	G1	49.00	822	0336	67	G5	783.99	13153	3361
20	G1$	51.91	871	0367	68	G5$	830.61	13935	366F
21	A1	55.00	923	039B	69	A5	880.00	14764	39AC
22	A1$	58.27	978	03D2	70	A5$	932.33	15642	3D1A
23	B1	61.74	1036	040C	71	B5	987.77	16572	40BC
24	C2	65.41	1097	0449	72	C6	1046.50	17557	4495
25	C2$	69.30	1163	048B	73	C6$	1108.73	18601	48A9
26	D2	73.42	1232	04D0	74	D6	1174.66	19709	4CFC
27	D2$	77.78	1305	0519	75	D6$	1244.51	20897	518F
28	E2	82.41	1383	0567	76	E6	1318.51	22121	5669
29	F2	87.31	1465	05B9	77	F6	1396.91	23436	5B8C
30	F2$	92.50	1552	0610	78	F6$	1479.98	24830	60FE
31	G2	98.00	1644	066C	79	G6	1567.98	26306	6602
32	G2$	103.83	1742	06CE	80	G6$	1661.22	27871	6CDF

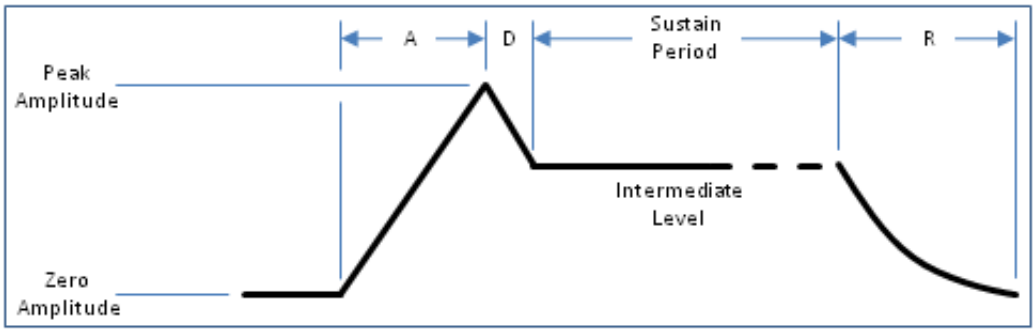
33	A2	110.00	1845	0735	81	A6	1760.00	29528	7358
34	A2$	116.54	1955	07A3	82	A6$	1864.65	31234	7A34
35	B2	123.47	2071	0817	83	B6	1975.53	33144	8178
36	C3	130.81	2195	0893	84	C7	2093.00	35115	892B
37	C3$	138.59	2325	0915	85	C7$	2217.46	37203	9153
38	D3	146.83	2463	099F	86	D7	2349.32	39415	99F7
39	D3$	155.56	2610	0A32	87	D7$	2489.01	41759	A31F
40	E3	164.81	2765	0ACD	88	E7	2637.02	44242	ACD2
41	F3	174.61	2930	0B72	89	F7	2793.83	46873	B719
42	F3$	185.00	3104	0C20	90	F7$	2959.95	49660	C1FC
43	G3	196.00	3288	0C08	91	G7	3135.96	52613	C085
44	G3$	207.65	3484	0D9C	92	G7$	3322.44	55741	0980
45	A3	220.00	3691	0E6B	93	A7	3520.00	59056	E6B0
46	A3$	233.08	3910	0F46	94	A7$	3729.31	62567	F467
47	B3	246.94	4143	102F	95	B7	3951.06	*66288	*1F2F0

Although the table above provides a simple and quick method for generating the equal-tempered scale, it is very memory inefficient as it requires 192 bytes for the table alone. Memory efficiency can be improved by determining the note value algorithmically. Using the fact that each note in an octave is exactly half the frequency of that note in the next octave, the note look-up table can be reduced from 96 entries to 12 entries, as there are 12 notes per octave. If the 12 entries (24 bytes) consist of the 16-bit values for the eighth octave (C7 through B7), then notes in lower octaves can be derived by choosing the appropriate note in the eighth octave and dividing the 16-bit value by two for each octave of difference. As division by two is nothing more than a right-shift of the value, the calculation can easily be accomplished by a simple software routine. Although note B7 is beyond the range of the Oscillators this value should still be included in the table for calculation purposes (the MSB of B7 would require a special software case, such as generating this bit in the CARRY before shifting). Each note must be specified in a form which indicates which of the 12 semitones is desired, and which of the eight octaves the semitone is in. Since four bits are necessary to select 1 of 12 semitones and three bits are necessary to select 1 of 8 octaves, the information can fit in one byte, with the lower nybble selecting the semitone (by addressing the look-up table) and the

upper nybble being used by the division routine to determine how many times the table value must be right-shifted.

Appendix B - SID Envelope Generators

The four-part ADSR (ATTACK, DECAY, SUSTAIN, RELEASE) envelope generator has been proven in electronic music to provide the optimum trade-off between flexibility and ease of amplitude control. Appropriate selection of envelope parameters allows the simulation of a wide range of percussion and sustained instruments. The violin is a good example of a sustained instrument. The violinist controls the volume by bowing the instrument. Typically, the volume builds slowly, reaches a peak, then drops to an intermediate level. The violinist can maintain this level for as long as desired, then the volume is allowed to slowly die away. A “snapshot” of this envelope is shown below:

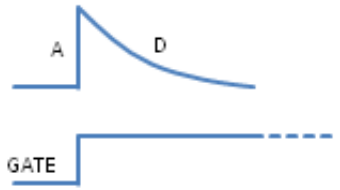


This volume envelope can be easily reproduced by the ADSR as shown below, with typical envelope rates:

Note that the tone can be held at the intermediate SUSTAIN level for as long as desired. The tone will not begin to die away until GATE is cleared. With minor alterations, this basic envelope can be used for brass and woodwinds as well as strings.

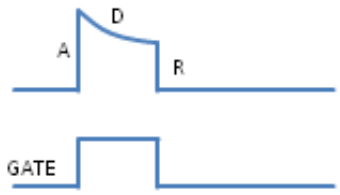
An entirely different form of envelope is produced by percussion instruments such as drums, cymbals and gongs, as well as certain keyboards such as pianos and harpsichords. The percussion envelope is characterized by a nearly instantaneous attack, immediately followed by a decay to zero volume. Percussion instruments cannot be sustained at a constant amplitude. For example, the instant a drum is struck, the sound reaches full volume and decays rapidly regardless of how it was struck. A typical cymbal envelope is shown below:

Attack:	0	2mS
Decay:	9	750mS
Sustain:	0	
Release:	9	750mS



Note that the tone immediately begins to decay to zero amplitude after the peak is reached, regardless of when GATE is cleared. The amplitude envelope of pianos and harpsichords is somewhat more complicated, but can be generated quite easily with the ADSR. These instruments reach full volume when a key is first struck. The amplitude immediately begins to die away slowly as long as the key remains depressed. If the key is released before the sound has fully died away, the amplitude will immediately drop to zero. This envelope is shown below:

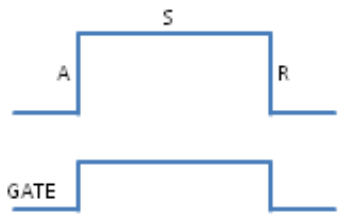
Attack:	0	2mS
Decay:	9	750mS
Sustain:	0	
Release:	0	6mS



Note that the tone decays slowly until GATE is cleared, at which point the amplitude drops rapidly to zero.

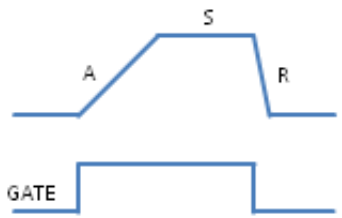
The most simple envelope is that of the organ. When a key is pressed, the tone immediately reaches full volume and remains there. When the key is released, the tone drops immediately to zero volume. This envelope is shown below:

Attack:	0	2mS
Decay:	0	6mS
Sustain:	15 ($F)	
Release:	0	6mS



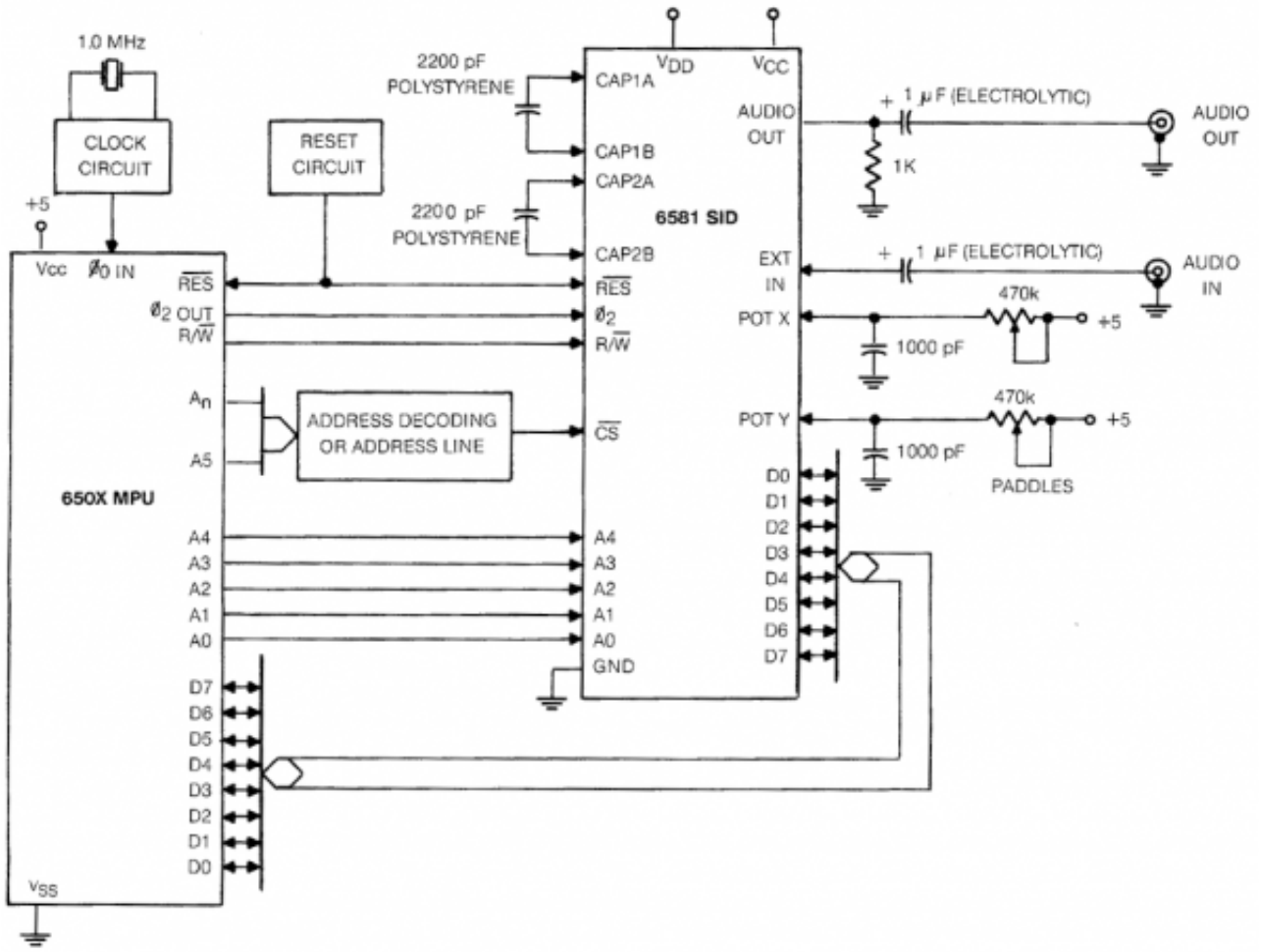
The real power of SID lies in the ability to create original sounds rather than simulations of acoustic instruments. The ADSR is capable of creating envelopes which do not correspond to any “real” instruments. A good example would be the “backwards” envelope. This envelope is characterized by a slow attack and rapid decay which sounds very much like an instrument that has been recorded on tape then played backwards. This envelope is shown below:

Attack:	10 ($A)	500mS
Decay:	0	6mS
Sustain:	15 ($F)	
Release:	3	72mS



Many unique sounds can be created by applying the amplitude envelope of one instrument to the harmonic structure of another. This produces sounds similar to familiar acoustic instruments, yet notably different. In general, sound is quite subjective and experimentation with various envelope rates and harmonic contents will be necessary in order to achieve the desired sound.

Appendix C - Typical 6581 SID Application



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OBSOLETE PRODUCT
RECOMMENDED REPLACEMENT PART
HFA3046

December 15, 2011 File Number 341.6

General Purpose NPN Transistor Array

The CA3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

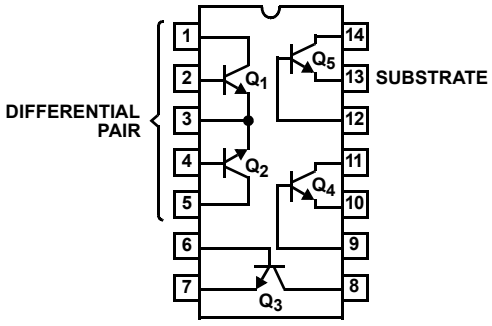
The transistors of the CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3046	-55 to 125	14 Ld PDIP	E14.3
CA3046M (3046)	-55 to 125	14 Ld SOIC	M14.15
CA3046M96 (3046)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA3046 (PDIP, SOIC)
TOP VIEW



Features

- Two Matched Transistors
  - V_{BE} Match . . . . . ±5mV
  - I_{IO} Match. . . . . .2μA (Max)
- Low Noise Figure . . . . . 3.2dB (Typ) at 1kHz
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Full Military Temperature Range

Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 “Application of the CA3018 Integrated-Circuit Transistor Array” for Suggested Applications

Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CEO}) 15V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 50mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	180	N/A
SOIC Package	220	N/A

Maximum Power Dissipation (Any One Transistor) 300mW
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25^oC$, characteristics apply for each transistor in CA3046 as specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$		5	7	-	V
Collector Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$		-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$		-	See Fig. 2	0.5	μA
Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3)	h_{FE}	$V_{CE} = 3V$	$I_C = 10mA$	-	100	-	-
			$I_C = 1mA$	40	100	-	-
			$I_C = 10\mu A$	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2. $\|I_{IO1} - I_{IO2}\|$ (Note 3) (Figure 4)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.3	2	μA
Base-to-Emitter Voltage (Note 3) (Figure 5)	V_{BE}	$V_{CE} = 3V$	$I_E = 1mA$	-	0.715	-	V
			$I_E = 10mA$	-	0.800	-	V
Magnitude of Input Offet Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$ (Note 3) (Figures 5, 7)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$ (Note 3) (Figures 5, 7)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3V$, $I_C = 1mA$		-	-1.9	-	$mV/^oC$
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$		-	0.23	-	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$	$V_{CE} = 3V$, $I_C = 1mA$		-	1.1	-	$\mu V/^oC$
DYNAMIC CHARACTERISTICS							
Low Frequency Noise Figure (Figure 9)	NF	f = 1kHz, $V_{CE} = 3V$, $I_C = 100\mu A$, Source Resistance = $1k\Omega$		-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics							
Forward Current Transfer Ratio (Figure 11)	h_{FE}	f = 1kHz, $V_{CE} = 3V$, $I_C = 1mA$		-	110	-	-
Short Circuit Input Impedance (Figure 11)	h_{IE}	f = 1kHz, $V_{CE} = 3V$, $I_C = 1mA$		-	3.5	-	$k\Omega$
Open Circuit Output Impedance (Figure 11)	h_{OE}	f = 1kHz, $V_{CE} = 3V$, $I_C = 1mA$		-	15.6	-	μS

LM2904,LM358/LM358A,LM258/ LM258A

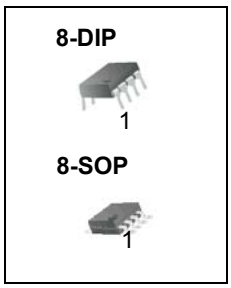
Dual Operational Amplifier

Features

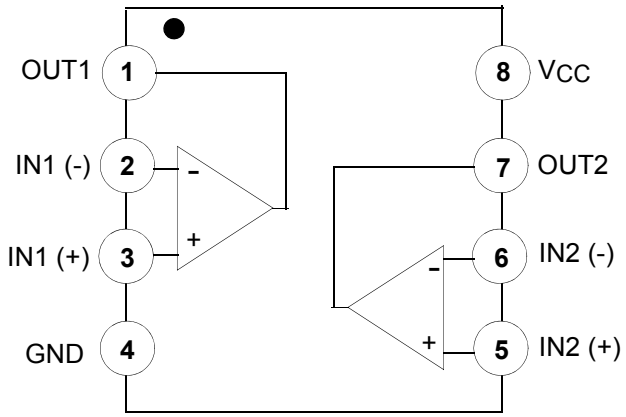
- Internally Frequency Compensated for Unity Gain
- Large DC Voltage Gain: 100dB
- Wide Power Supply Range:
  LM258/LM258A, LM358/LM358A: 3V~32V (or ±1.5V ~ 16V)
  LM2904 : 3V~26V (or ±1.5V ~ 13V)
- Input Common Mode Voltage Range Includes Ground
- Large Output Voltage Swing: 0V DC to Vcc -1.5V DC
- Power Drain Suitable for Battery Operation.

Description

The LM2904,LM358/LM358A, LM258/LM258A consist of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP-AMP circuits which now can be easily implemented in single power supply systems.



Internal Block Diagram



Electrical Characteristics (Continued)

(V_{CC}= 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of -25°C ≤ T_A ≤ +85°C for the LM258; and the 0°C ≤ T_A ≤ +70°C for the LM358; and the -40°C ≤ T_A ≤ +85°C for the LM2904

Parameter	Symbol	Conditions	LM258			LM358			LM2904			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} -1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω	-	-	7.0	-	-	9.0	-	-	10.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S = 0Ω	-	7.0	-	-	7.0	-	-	7.0	-	μV/°C
Input Offset Current	I_{IO}	-	-	-	100	-	-	150	-	45	200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	-	-	10	-	-	10	-	-	10	-	pA/°C
Input Bias Current	I_{BIAS}	-	-	40	300	-	40	500	-	40	500	nA
Input Voltage Range	$V_{I(R)}$	V_{CC} = 30V (LM2904 , V_{CC} = 26V)	0	-	V_{CC} -2.0	0	-	V_{CC} -2.0	0	-	V_{CC} -2.0	V
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L =2.0kΩ $V_{O(P)}$ = 1V to 11V	25	-	-	15	-	-	15	-	-	V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC}=30V (V_{CC} = 26V for LM2904) R_L = 2kΩ	26	-	-	26	-	-	22	-	-	V
		R_L=10kΩ	27	28	-	27	28	-	23	24	-	V
	$V_{O(L)}$	V_{CC} = 5V, R_L=10kΩ	-	5	20	-	5	20	-	5	20	mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V, V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30	-	10	30	-	10	30	-	mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V, V_{CC} = 15V, $V_{O(P)}$ = 2V	5	8	-	5	9	-	5	9	-	mA
Differential Input Voltage	$V_{I(DIFF)}$	-	-	-	V_{CC}	-	-	V_{CC}	-	-	V_{CC}	V

BRICKED ARDUINO MEGA

EXIT ARDUINO PROGRAM

TURN OFF POWER TO THE MEGA FOR A MINUTE

TURN BACK ON

START UP ARDUINO PROGRAM
FROM “TOOLS” MENU CHECK THAT MEGA USB IS GOOD

OPEN THE “BLINK” PROGRAM

PRESS THE LOAD BUTTON

RIGHT BEFORE THE COMPILE BAR FINISHES, PRESS AND RELEASE THE RESET