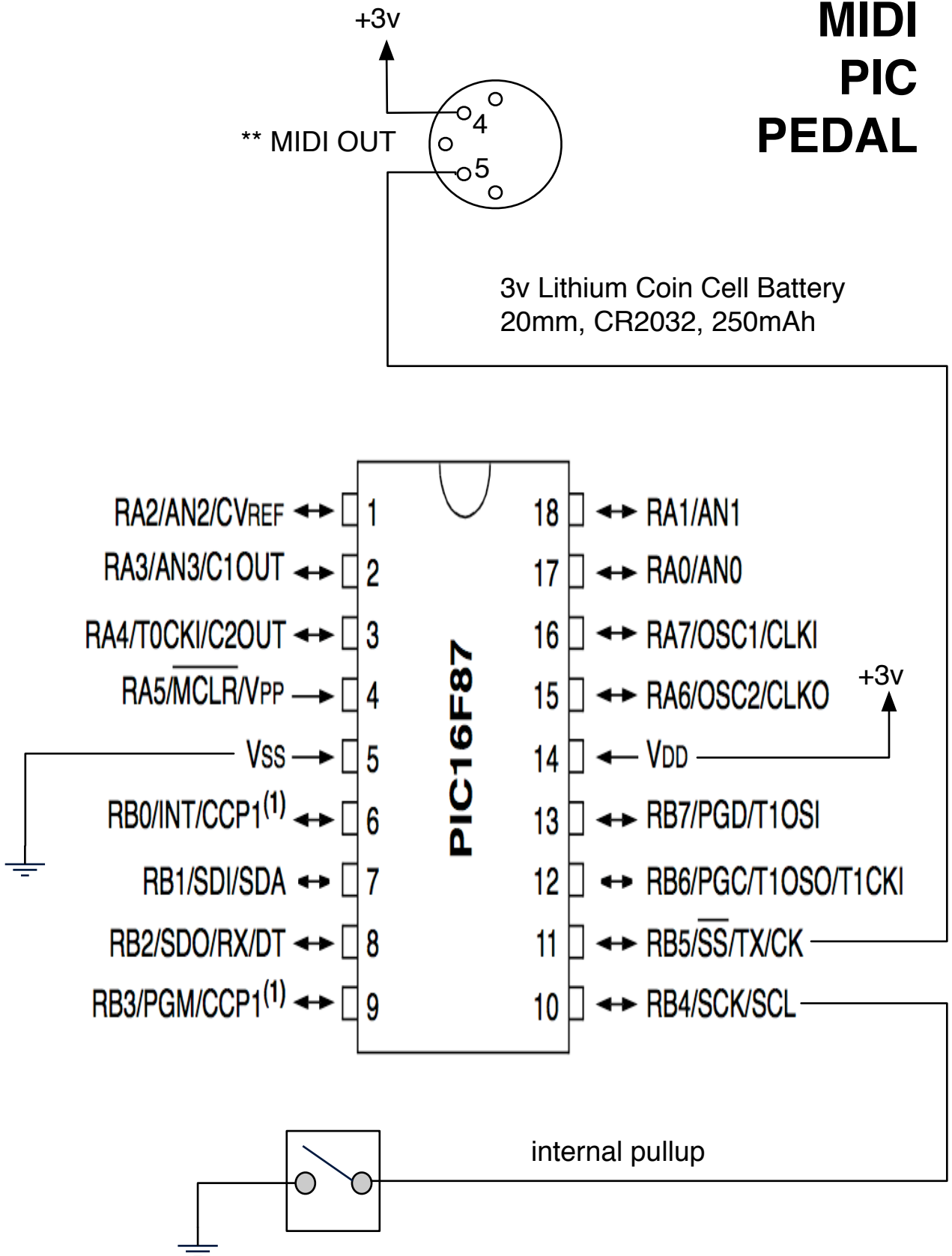


MIDI PIC PEDAL



** No 220Ω resistors on the MIDI lines because of 3v operation and 70Ω Thevenin equivalent resistance on low pic output lines.

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1  ; _____ PIC16F87 MIDI FOOT PEDAL PROJECT _____
2  ;MIDI Note-On (Off is Note-On with zero velocity) transmitted from one pedal switch.
3  ;
4  ;RB5 = TX used as MIDI Out. From the internal AUSART serial transmitter.
5  ;
6  ;RB4 = Switch Input, with the internal weak-pull-up enabled. "PORTB Change Interrupts" enabled
7  ;so that any activity on RB4 will wake up the processor and start the interrupt routine "main". The
8  ;processor sleeps with very low power consumption inbetween pedal activity.
9  ;
10 ;Use INTIO1, internal 8MHz clock, check RA6 for 8MHz/4, can be tweaked with OSCTUNE Reg.
11 ;Load SPBRG with 15 (decimal) for a baud rate of 31.25KHz (Midi Rate) = 8MHz/(16(x+1))
12 ;
13 ; -----
14     list    p=16F87
15 ;
16 ;         CONFIGURATION BITS set in MPLab:
17 ;
18 ;         OSC = INTIO1, INTRC-OSC2 as Clock Out
19 ;         Watchdog Timer = Off
20 ;         Power Up Timer = Off
21 ;         Brown Out Detect = Off
22 ;         Low Voltage Program = Off
23 ;         Data EE Read Protect = Off
24 ;         Flash Program Write Protect = Off
25 ;         Code Protect = Off
26 ;         Fail-Safe Clock Mon. Enb = Disabled
27 ;         Internal Ext. Switch Over Mode = Disabled
28 ;
29 MOVLF    macro    literal, dest
30         movlw    literal
31         movwf    dest
32     endm
33 ; -----
34 ; VARIABLES -- STORED IN REGISTERS ABOVE THE DEDICATED REGISTERS
35 ; -----
36         cblock    0x20
37
38             vel                ;holds 0 for note off or MIDI_VEL for note on
39             x                    ;delay register
40             y                    ;delay register
41
42         endc
43 ; -----
44 ;         USEFUL EQUATES (Some not used here, mentioned for future programs)
45 ; -----
46
47 PORTA    equ        H'0005'

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48 PORTB    equ    H'0006'
49 TRISA    equ    H'0085'    ;Data Direction for PORTA
50 TRISB    equ    H'0086'    ;Data Direction for PORTB
51 STATUS   equ    H'0003'
52 PCL      equ    H'0002'    ;Low Program Counter
53 OPTION_REG equ    H'0081'    ;Option Control Reg.
54
55 ; -----AUSART Registers-----
56 TXSTA    equ    H'0098'    ;Transmit Status and Control Reg.
57 RCSTA    equ    H'0018'    ;Receive Status and Control Reg.
58 SPBRG    equ    H'0099'    ;Baud Rate Generator for AUSART
59 TXREG    equ    H'0019'    ;Transmit Data Reg.
60 RCREG    equ    H'001A'    ;Receive Data Reg.
61
62 ; -----Internal OSC Registers-----
63 OSCCON   equ    H'008F'    ;OSC Control Reg.
64 OSCTUNE  equ    H'0090'    ;OSC Tuning of Internal clock
65
66 ; -----Interrupt Control Registers-----
67 INTCON   equ    H'000B'    ;Interrupt Control Reg.
68 PIE1    equ    H'008C'    ;Peripheral Interrupt Enable Reg1
69 PIE2    equ    H'008D'    ;Peripheral Interrupt Enable Reg2
70 PIR1    equ    H'000C'    ;Peripheral Interrupt Request Flags
71
72 ; -----Individual Bits of Registers Above-----
73 RP0     equ    H'05'    ;Bank Select bit in STATUS
74 C       equ    H'00'    ;Carry bit in STATUS
75 Z       equ    H'02'    ;Zero bit in STATUS
76 TXIF    equ    H'04'    ;PIR1 Reg. Reads 1 when TXREG is empty i.e.
77         ;TSR loaded. Cleared by loading TXREG.
78 TRMT    equ    H'01'    ;TXSTA Reg. 1=TSR empty, 0=TSR full
79         ;TSR is the Transmit Shift Register.
80 RCIF    equ    H'05'    ;PIR1 Reg. Reads 1 when RCREG is full ?
81         ;byte received. Cleared by reading RCREG.
82 ADIF    equ    H'06'    ;PIR1 Reg. Reads 1 when A/D convert is done.
83         ;Cleared in software.
84 TMR1IF  equ    H'00'    ;PIR1 Reg. Reads 1 when TMR1 overflows
85         ;Cleared in software.
86 GIE     equ    H'07'    ;INTCON reg. Global Interrupt Enable
87 RBIE    equ    H'03'    ;INTCON reg. RB port change interrupt enable
88 RBIF    equ    H'00'    ;INTCON reg. RB port change interrupt flag
89
90
91 ; -----Other values -----
92 F       equ    H'01'    ;Instruction results go to the specified register
93 W       equ    H'00'    ;Instruction results go to W
94 NOTE_ON equ    H'90'    ;MIDI Status byte - NoteOn, Chnl 0 (low nibble)

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95 PEDAL_IN equ H'04' ;Pedal Switch connected to RB4
96 MIDI_KEY equ H'30' ;MIDI key value 00 thru 7F (arbitrary)
97 MIDI_VEL equ H'60' ;MIDI Note Velocity (arbitrary)
98 ;-----
99
100 org 0x0000 ;Reset/PowerUp vector
101 goto initialize
102
103 org 0x0004
104 goto main ;Interrupt Routine vector, GIE disabled
105 ;
106 ;-----
107 ; INITIALIZE Control Registers
108 ;-----
109 initialize MOVLF B'00000000', PIR1 ;Clear Periph Interrupt Request Flags
110 MOVLF B'10000000', RCSTA ;Enable UART
111
112 bsf STATUS, RP0 ;switch to bank 1
113 ;
114 MOVLF B'11111111', TRISA ;Port A is all inputs
115 MOVLF B'00010000', TRISB ;RB5=TX, RB4=pedal in
116 MOVLF B'01111100', OSCCON ;OSC Control Reg
117 MOVLF B'00000000', OSCTUNE ;OSC Tune the 8MHz internal clock
118 MOVLF B'00000000', OPTION_REG ;Enables PORTB pull-ups
119 MOVLF B'00000000', PIE1 ;Disable peripheral interrupt
120 MOVLF B'00000000', PIE2 ;Disable peripheral interrupts
121 MOVLF B'10100110', TXSTA ;Set up Transmit 8-bit, asynch, hi-speed
122 MOVLF B'00001111', SPBRG ;Set Transmit Baud Rate to 31.25KHz
123 ;
124 bcf STATUS, RP0 ;switch back to bank 0
125
126 MOVLF B'10001000', INTCON ;Enable "RB port change" interrupts
127 ;GIE and RBIE enables set
128 sleep_again sleep
129 goto sleep_again ;power down till pedal changes
130
131 ;-----
132 ; MAIN INTERRUPT ROUTINE (RBIF flag interrupt - the only kind enabled)
133 ;-----
134 main MOVLF vel, MIDI_VEL ;Setting Key Velocity
135 btfss PORTB, 4 ;If pedal switch is 0, Then key vel = 0
136 ;(to switch polarity use btfsc instead)
137 clrf vel ; Else key velocity = MIDI_VEL
138 call midi_tx ;Call the Transmit Subroutine
139 bcf INTCON, RBIF ;Clear RB port change interrupt f
140 retfie ;GIE re-enabled for interrupts
141

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142
143 ;-----
144 ;           SUBROUTINE FOR TRANSMITTING MIDI NOTE ON
145 ;-----
146 midi_tx    MOVLF    NOTE_ON, TXREG    ;Send the MIDI Note-On Status Byte
147           MOVLF    1, x              ;delay 0.39ms
148           call     delay
149           MOVLF    MIDI_KEY, TXREG    ;Send the MIDI Note-On Key value
150           MOVLF    1, x              ;delay 0.39ms
151           call     delay
152           MOVLF    vel, TXREG         ;Send the MIDI Note-On Key Velocity
153           MOVLF    0x33, x           ;Delay 20ms for switch debouncing
154           call     delay
155           return
156
157 ;
158 ;-----
159 ;           SUBROUTINE FOR DELAY
160 ; With y=255, x=1 is 0.39ms, x=3 is 1.2ms, x=8 is 3ms, x=16 is 6ms, x=51 is 20ms
161 ;-----
162 delay      nop                    ;Delay = (3xy+5x+6)(1/2MHz) seconds
163 outer_loop MOVLF    0xff, y
164 inner_loop decfsz   y, F
165           goto     inner_loop
166           decfsz   x, F
167           goto     outer_loop
168           return
169 ;-----
170           end
171
172
173
174
175
176 ; John Talbert, Oberlin Conservatory, May, 2009
177
178
179

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